

National Exams

98-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.
2. This is a OPEN BOOK exam.
Any non-communicating calculator is permitted.
3. FIVE (5) questions constitute a complete exam paper.
The first 5 questions as they appear in the answer book will be marked.
4. Each question is of equal value.

Question 1 (20 marks)

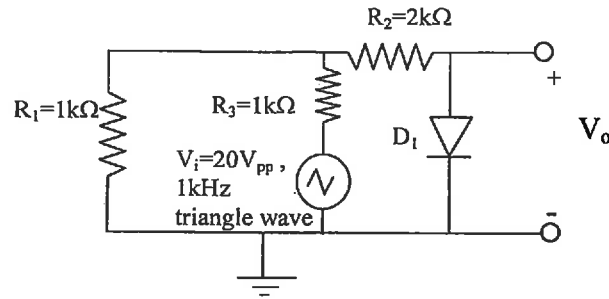


Figure 1. The diode can be replaced by piece-wise linear model with $V_D=0.7V$, $R_S=10\Omega$ for forward bias.

For the circuit shown in Figure 1:

- Sketch V_i and V_o as a function of time, indicating peak voltages.
- What is the peak reverse voltage across D_1 ?
- What is the peak power dissipated in D_1 ?

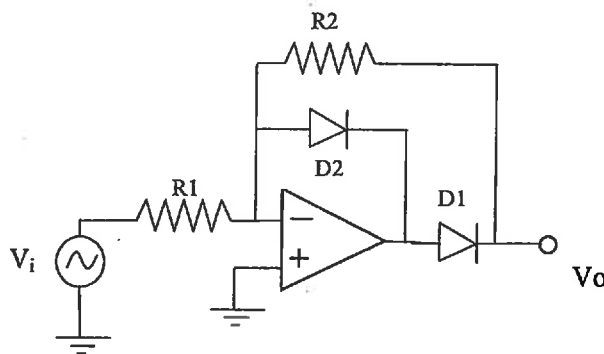


Figure 2. Assume the diodes have a voltage drop $V_D=0.7V$ when conducting. $R_1=R_2=1k\Omega$.

For the circuit shown in Figure 2:

- For $V_i=10V \sin(2\pi 60t)$ sketch the output $V_o(t)$. Label key voltages and times, and indicate changes in operating region for each diode.

Question 2 (20 marks)

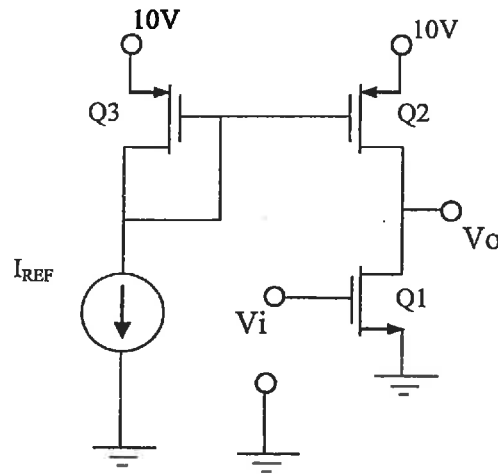


Figure 3. $k_n' = \mu_n C_{ox} = 1 \text{ mA/V}^2$, $k_p' = 40 \text{ } \mu\text{A/V}^2$, $W/L = 10 \text{ } \mu\text{m}$, $V_{tn} = -V_{tp} = 1\text{V}$, $|V_A| = 100\text{V}$

For the circuit shown in Figure 3:

- a) Draw a small signal ac equivalent circuit.
- b) Find an expression for voltage gain V_o/V_i .
- c) Choose a bias current I_{REF} to provide a gain of 200 V/V.
- d) A load resistor of 100 k Ω is connected from V_o to ground. What is the voltage gain?

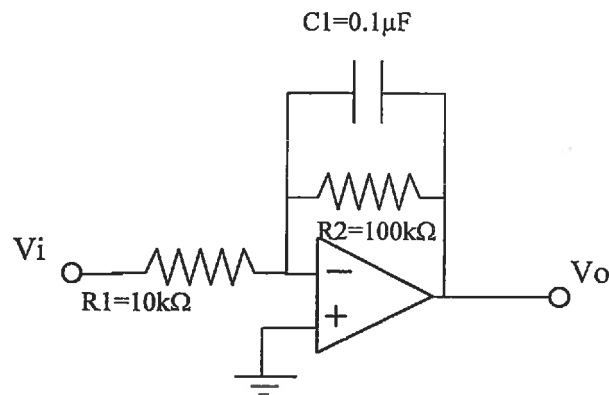
Question 3 (20 marks)

Figure 4.

For the circuit shown in Figure 4:

- Derive the transfer function $\frac{V_o(j\omega)}{V_i(j\omega)}$ for the circuit shown, assuming the op-amp is ideal.
- Find the DC gain, 3dB frequency, and the unity gain bandwidth for this circuit.
- If $V_i(t) = 1\sin(200t)$ V, find $V_o(t)$.
- If the op-amp has a finite gain $A = 10^4$ V/V, find the transfer function $\frac{V_o(j\omega)}{V_i(j\omega)}$.

Question 4(20 marks)

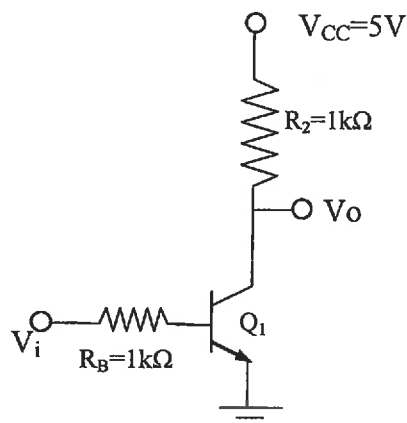


Figure 5. $V_{be}=0.7V$ (active), $V_{ce}=0.2V$ (saturation), $\beta=100$.

For the circuit shown in Figure 5:

- What value of V_i will make Q_1 active? What is the expression for V_o for this input?
- What value of V_i will make Q_1 saturate?
- For Q_1 active with $I_C=1mA$, draw the small signal AC equivalent circuit. Evaluate the voltage gain.

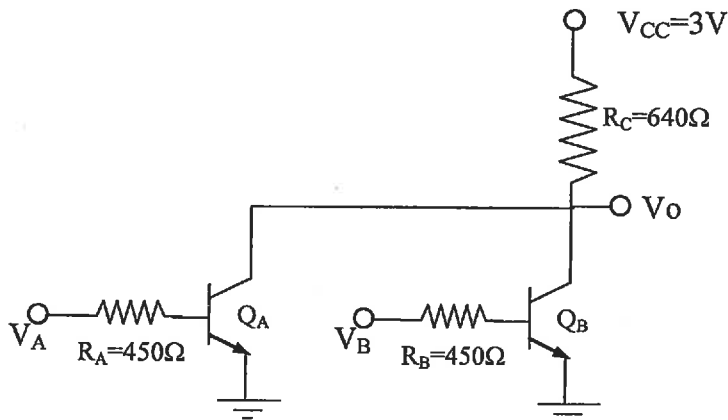


Figure 6. $V_{be}=0.7V$ (active), $V_{ce}=0.2V$ (saturation), $\beta=100$.

- For $V_A=V_B=0V$, what is the state of each transistor and the value of V_o ?
- For V_A or $V_B=3V$, what is the state of each transistor and the value of V_o ?

Question 5 (20 marks)

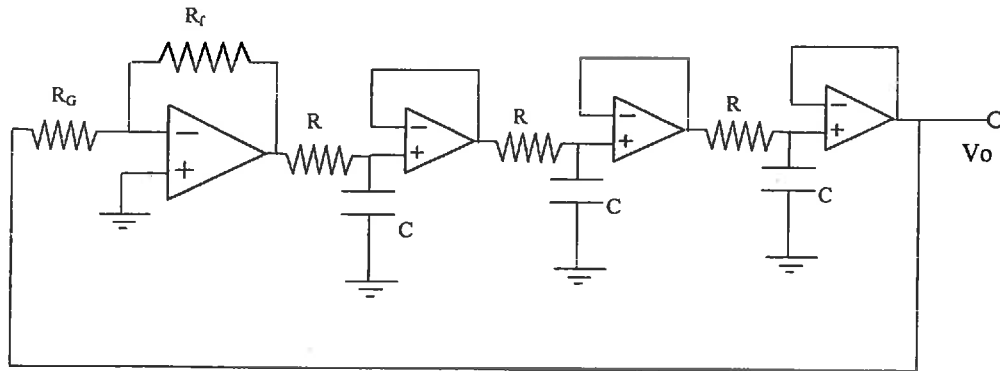


Figure 7. Assume the op-amps are ideal. $R=10\text{k}\Omega$, $R_f=100\text{k}\Omega$

For the circuit shown in Figure 7:

- Find the loop gain expression.
- What condition on the loop gain will result in oscillation? What is the expression for oscillation frequency for this circuit?
- Choose a value R_G that will initiate oscillation.
- Choose a value C to provide an oscillation frequency of 1kHz.

Question 6 (20 marks)

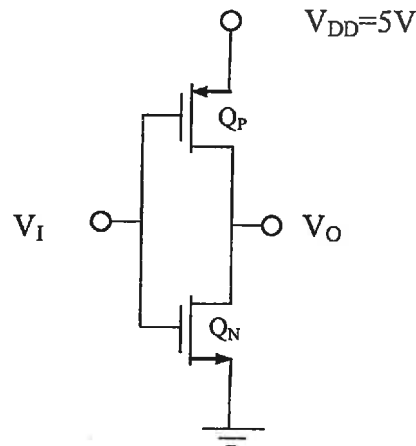


Figure 8. $k_n' = 50 \mu\text{A}/\text{V}^2$, $k_p' = 20 \mu\text{A}/\text{V}^2$, $V_{tn} = -V_{tp} = 1\text{V}$, $C_{ox} = 1\text{fF}/\mu\text{m}^2$

- a) If the minimum gate length for this technology is $1 \mu\text{m}$, size Q_N and Q_P to obtain a symmetric transfer characteristic.
- b) Estimate the propagation delay if the inverter drives a second identical inverter. Consider only the gate oxide contribution to capacitance.

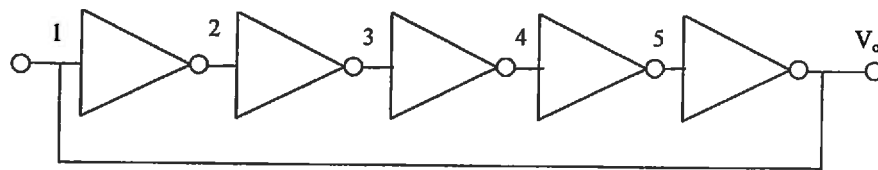


Figure 9.

For the circuit shown in Figure 9:

- c) For a low to high transition at node 1 at $t=0\text{s}$, sketch the waveforms at all 5 nodes for one full period.
- d) If the propagation delay for a single inverter is 0.5 ns , what is the frequency of the signal supplied by this circuit?

Question 7 (20 marks)

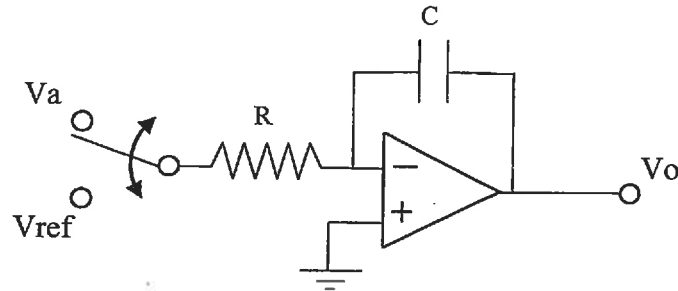


Figure 10.

- Initial value of $V_o = 0V$. At $t=0s$ the switch is connected to V_a (negative). What is $V_o(t)$?
- At $t=T_1$ S is moved to connect to V_{ref} (positive). How long (T_2) will it take for V_o to return to $0V$?
- A counter measures T_1 and T_2 . If the counter value is n_{ref} at $t=T_1$, what is the value at $t=T_2$?
- If $V_{ref} = 10V$ and $n_{ref} = 2^8$, what is the voltage resolution in measuring V_a ?

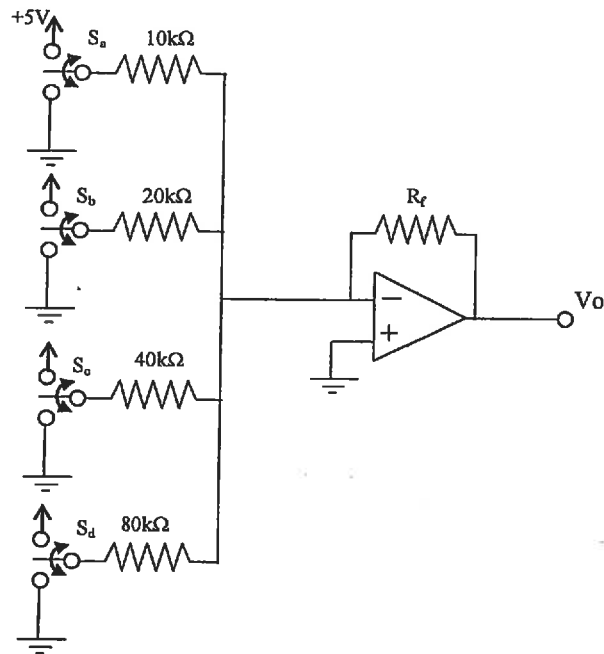


Figure 11.

- For the circuit in Figure 11, find the expression for V_o as a function of switch positions S_a to S_d . Which switch represents the most significant bit?

Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total (4 parts, 5 marks each)
3. 20 marks total (4 parts, 5 marks each)
4. 20 marks total (a),b),c) 5 marks each, d) 2 marks, e) 3 marks)
5. 20 marks total (4 parts, 5 marks each)
6. 20 marks total (4 parts, 5 marks each)
7. 20 marks total (a) 4 marks, b) 4 marks, c) 3 marks, d) 4 marks, e) 5 marks)