NATIONAL EXAMS
MAY 2012

Phys-A5: Semiconductor Devices & Circuits

3 hours duration

NOTES:

1. If doubt exits as to the interpretation of any question, the candidate must submit with the answer paper, a clear statement of any assumption made.

2. Candidates may use one of two calculators, the Casio or Sharp approved models.

3. This is a CLOSED BOOK EXAM.
   Useful constants and equations have been annexed to the exam paper.

4. **Any FIVE (5) of the SEVEN (7)** questions constitute a complete exam paper.
   The first five questions as they appear in the answer book will be marked.

5. When answering questions, candidates must clearly indicate units for all parameters used or computed.

1. A sample of pure silicon (Si) is maintained at a temperature of 300 °K. At this temperature, this semiconductor has a band gap of 1.1 eV.

3 pts (a) What is the intrinsic hole concentration p_i in the Si sample?

3 pts (b) Find the separation between the intrinsic level E_i and the valence band level E_v.

(c) If this sample is doped with 10^{17} donor atoms/cm^3,

7 pts i. what is the equilibrium hole concentration in the sample?

7 pts ii. what is the energy separation between the Fermi level and the conduction band level?

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2. An abrupt silicon *p-n* junction is formed by merging p-type and n-type semiconductors of constant cross section A = 10^{-4} cm^2 which have the following properties at a temperature of T = 300 °K:

p type	***n type***
$N_a = 10^{17}$ cm^{-3}	$N_d = 10^{15}$ cm^{-3}
$\tau_n = 0.1$ μs	$\tau_p = 10$ μs
$\mu_p = 200$ cm^2/(V-s)	$\mu_n = 1300$ cm^2/(V-s)
$\mu_n = 700$ cm^2/(V-s)	$\mu_p = 450$ cm^2/(V-s)

This *p-n* junction is used as a diode in the circuit shown in Figure P2 where the diode forward bias voltage V is obtained by using a battery and a resistor R.

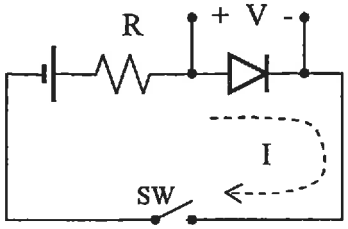

Figure P2

6 pts (a) When switch SW is open, what is the value of the depletion region in the diode?

4 pts (b) When the switch is closed, a current I flows in the circuit. Briefly explain if inside the diode this current is due to drift or diffusion.

(c) If the battery and the resistor R are chosen to set the value of the diode voltage V at +0.7 V,

7 pts i. what is the value of current I in this situation?

3 pts ii. what happens to the depletion region compared to case (a)?

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3. A basic passive filter is shown in Figure P3.

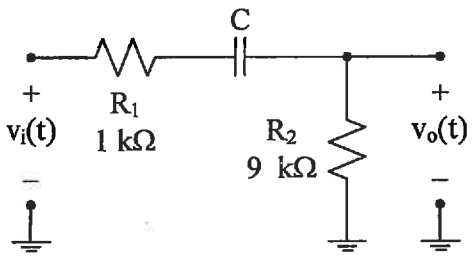

Figure P3

5 pts (a) Show that the transfer function $F(s) \equiv V_o(s)/V_i(s)$ of the filter can be expressed as

$$F(s) = \frac{R_2/(R_1 + R_2)}{1 + \dfrac{1}{s(R_1 + R_2)C}}$$

4 pts (b) If the input signal $v_i(t)$ is a very high frequency sinusoidal signal of amplitude equal to 5 V, what is the amplitude of the sinusoidal output signal $v_o(t)$?

5 pts (c) What must be the value of capacitor C to set the cut-off frequency of the filter at $f_{3dB} = 100$ Hz?

6 pts (d) If the value of the capacitor is set to C = 83 nF, what will be the value (in **dB**) of the magnitude $|F(s)|$ of $F(s)$ at a frequency of $\omega = 400$ rad/s.

4. The circuits shown in Figure P4a and Figure P4b are used to meet the requirement of a small signal amplifier. Assuming ideal resistors and ideal OP amps, the two circuits have the same input impedance R_{in} = 1 kΩ.

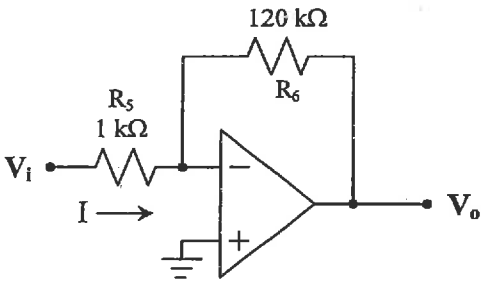

Figure P4a

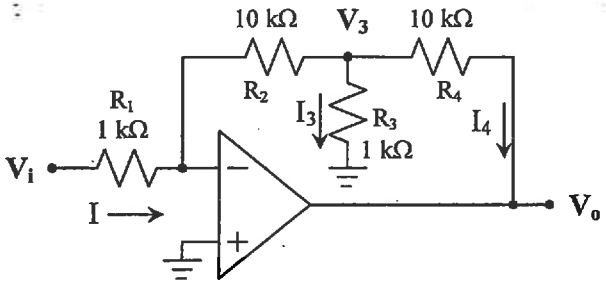

Figure P4b

6 pts (a) Show that the gain of the amplifier in Figure P4b is given by

$$\frac{V_o}{V_i} = -\left[\frac{R_2}{R_1} + \frac{R_4}{R_1} + \frac{R_2}{R_1}\frac{R_4}{R_3}\right]$$

4 pts (b) Show that both circuits have a gain equal to -120.

(c) It is now required to increase the input impedance of both circuits to a value of R_{in} = 50 kΩ, without changing the gain and without using resistors greater than 200 kΩ.

4 pts i. Explain why these requirements cannot be met by the circuit of Figure P4a.

6 pts ii. By using resistors as large as possible, select suitable resistor values for the circuit of Figure P4b to meet the specified requirements.

5. Figure P5 shows a binary inverter circuit and its voltage transfer characteristic (VTC) response.

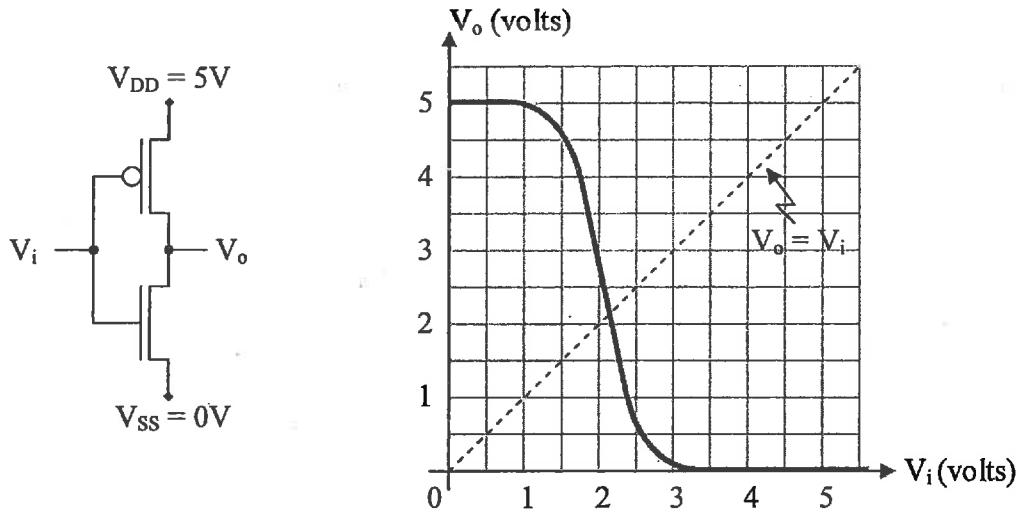

Figure P5

4 pts (a) What are the voltage values of the two logic levels of this binary circuit?

6 pts (b) From the VTC curve, extract approximate values of V_{IL} and V_{IH}, and calculate the noise margins NM_H and NM_L of this logic gate.

10 pts (c) If $V_{tn} = -V_{tp} = 1$ V and $k_n = 2k_p$, calculate the exact value of V_i when $V_i = V_o$.

6. Figure P6 shows the basic diagram of an N-bit flash analog-to-digital converter (ADC). The design of a 4-bit ADC is to be considered when the range of the analog input voltage is $0 \le V_A \le +10$ V.

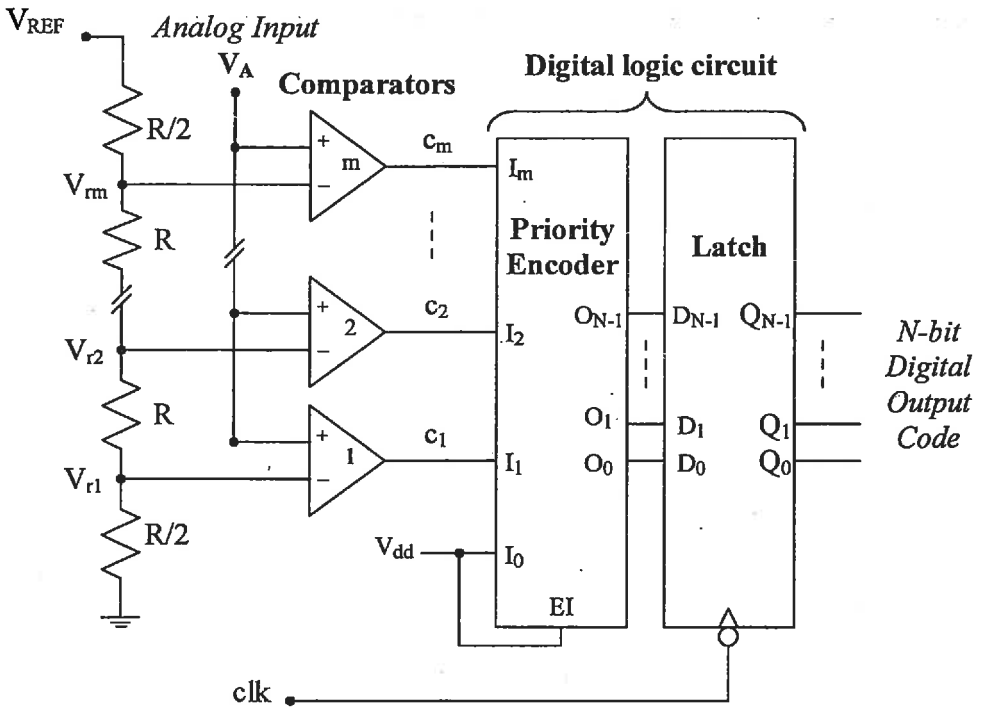

Figure P6

2 pts (a) Name one advantage and one disadvantage of this type of ADC?

2 pts (b) Calculate the number of comparators required for a 4-bit design?

2 pts (c) For a 4-bit design, if each comparator has a delay of 30 ns and the digital logic circuit has a maximum delay of 20 ns, what is the maximum conversion rate of the ADC?

4 pts (d) For the given input range, what is the resolution (in volts) of the 4-bit ADC?

6 pts (e) If $V_{REF} = +10$ V, what is the 4-bit output code when $V_A = 5.1$ V?

4 pts (f) What is the quantization error (in volts) for case (e)?

7. Figure P7 shows the basic diagram of a precision bridge rectifier for instrumentation applications. The OP amp is assumed to be ideal. The meter M has a coil resistance of r = 100 Ω and provides a full-scale deflection when the average current through it is 3.18 mA.

8 pts (a) Find the value of R to provide a full-scale reading when the input voltage is a sine wave of amplitude equal to 5 V.

8 pts (b) Assuming the diodes have a constant 0.5 V drop when conducting, what is the maximum positive voltage that can appear at the output of the OP amp?

4 pts (c) If an engineer decides to use diodes with a peak reverse voltage (PRV) rating equal to 2 V, will this rating be sufficient to prevent junction breakdown?

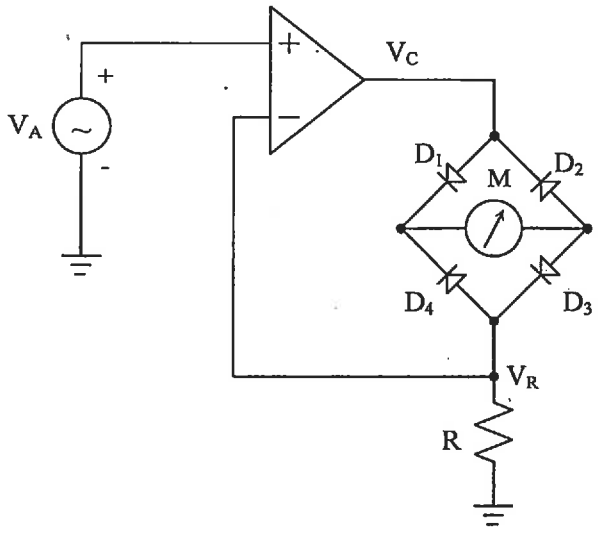

Figure P7

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ANNEX A

USEFUL CONSTANTS AND EQUATIONS

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(1) Ratio $|V_2/V_1|$ in dB = 20 log ($|V_2/V_1|$)

(2) $q = 1.6\times10^{-19}$ C

(3) $k = 1.38 \times 10^{-23}$ J/°K = 8.62×10^{-5} eV/°K [At T = 300°K, kT/q ≈ 26 mV kT = 0.026 eV]

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(4) For silicon (Si) at T = 300 °K: $n_i = 1.5\times10^{10}/cm^3$

(5) $\varepsilon_{Si} = 1.04\times10^{-12}$ F/cm

(6) $\varepsilon_{SiO2} = 0.345\times10^{-12}$ F/cm [farad: 1 F = 1 C/V] [siemens: 1 mS = 1 mA/V = 1 mmho]

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(7) $$f(E) = \frac{1}{1+e^{(E-E_F)/kT}}$$

(8) $$n_o + N_a = p_o + N_d$$

(9) $$n_o p_o = n_i^2$$

(10) $$n_o = N_c e^{(E_F-E_c)/kT} = n_i e^{(E_F-E_i)/kT}$$

(11) $$p_o = N_v e^{(E_v-E_F)/kT} = n_i e^{(E_i-E_F)/kT}$$

(12) $$n_i = \sqrt{N_c N_v}\, e^{-E_g/2kT}$$

(13) $$V_o = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$$

(14) $$W = \sqrt{\frac{2\varepsilon_{Si} V_o}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)}$$

(15) $$x_{po} = \frac{W N_d}{N_a + N_d} \qquad x_{no} = \frac{W N_a}{N_a + N_d}$$

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(16) $$\sigma = q(n_o\mu_n + p_o\mu_p)$$

(17) $$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{kT}{q} \qquad L_n = \sqrt{D_n \tau_n} \qquad L_p = \sqrt{D_p \tau_p}$$

(18) $$n_n p_n = n_i^2 = n_p p_p$$

(19) $$I = I_o(e^{\frac{qV}{kT}} - 1) = qA\left(\frac{D_p}{L_p} p_n + \frac{D_n}{L_n} n_p\right)(e^{\frac{qV}{kT}} - 1)$$

(20) $$J = \frac{I}{A} = \sigma \mathcal{E}$$

(21) $$R = \frac{L}{\sigma A}$$

MOS relationships and model

(22) $C_i = \dfrac{\varepsilon_{SiO_2}}{d}$

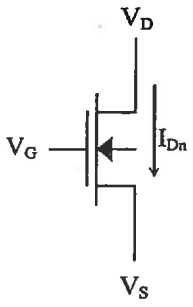
(23) $V_T = \Phi_{ms} + 2\phi_F - \dfrac{1}{C_i}(Q_i + Q_d)$

(24) $I_{Dn} = (k_n/2)\,(V_{GSn} - V_{tn})^2$ when $V_{DSn} > V_{GSn} - V_{tn}$

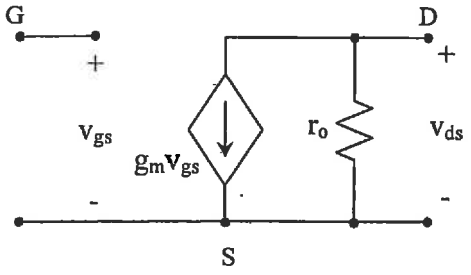
(25) $I_{Dn} = (k_n/2)\,[2(V_{GSn} - V_{tn})(V_{DSn}) - (V_{DSn})^2]$ when $V_{DSn} < V_{GSn} - V_{tn}$

(26) $I_{Dp} = -(k_p/2)\,(V_{GSp} - V_{tp})^2$ when $V_{DSp} < V_{GSp} - V_{tp}$

(27) $I_{Dp} = -(k_p/2)\,[2(V_{GSp} - V_{tp})(V_{DSp}) - (V_{DSp})^2]$ when $V_{DSp} > V_{GSp} - V_{tp}$



Small signal MOSFET model



Average and rms values

(28) $V_{DC} \equiv V_{average} = \dfrac{1}{T}\int_0^T V(t)\,dt$

[for a half-wave rectified sinewave $V(t) = V_p \sin \omega t$ of period T, $V_{average} = V_p/\pi$]

[for a full-wave rectified sinewave $V(t) = V_p \sin \omega t$ of period T, $V_{average} = 2V_p/\pi$]

(29) $V_{rms} = \sqrt{\dfrac{1}{T}\int_0^T [V(t)]^2\,dt}$

[for a half-wave rectified sinewave $V(t) = V_p \sin \omega t$ of period T, $V_{rms} = \dfrac{V_p}{2}$]

[for a full-wave rectified sinewave $V(t) = V_p \sin \omega t$ of period T, $V_{rms} = \dfrac{V_p}{\sqrt{2}}$]