# National Exams May 2012

## 07-Elec-A4, Digital Systems & Computers

3 hours duration

## NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

## Marking Scheme

1. (a) 2, (b) 5, (c) 2, (d) 3, total = 12
2. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
3. (a) 2.5, (b) 1.5, (c) 3, (d) 2, (e) 3, total = 12
4. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
5. (a) 4, (b) 4, (c) 4, total = 12
6. (a) 4, (b) 4, (c) 4, total = 12

The number beside each part above indicates the points that part is worth

**1.-** Given the following function in sums-of-product (SoP) form:

$$f(A,B,C,D) = \sum m_i(0,1,2,4,5,6,7,8,10)$$

where $m_i$ represent the minterms involved in the SoP canonical form of *f*.

(a) Prepare its truth table.

(b) Map the function $f$ in a K-map and identify:

i. One implicant that is not a prime implicant,

ii. One prime implicant that is not essential, and

iii. All essential prime implicants.

In identifying each implicant above list all the minterms in each of them.

(c) Write the minimized SoP form for *f*.

(d) Is the minimized SoP expression found hazard-free?
Explain and if it is not provide the hazard-free SoP form for *f*.

**2.-** Design a sequential circuit with two JK flip-flops, A and B, and two inputs E and X that performs as follows:

- If E = 0 the circuit remains in the same state regardless the value of X,
- When E = 1 and X = 1 the circuit goes through the state transitions AB = 00 to 01 to 10 to 11 back to 00, and repeats,
- When E = 1 and X = 0 the circuit goes through the state transitions AB = 00 to 11 to 10 to 01 back to 00, and repeats.

Provide:

(a) the state transition diagram,

(b) the state transition table,

(c) the K-map simplification of the combinational logic required, as well as

(d) a drawing of the resulting logic circuit diagram.

*Note*: Consult flip-flop excitation tables attached at the end as needed.

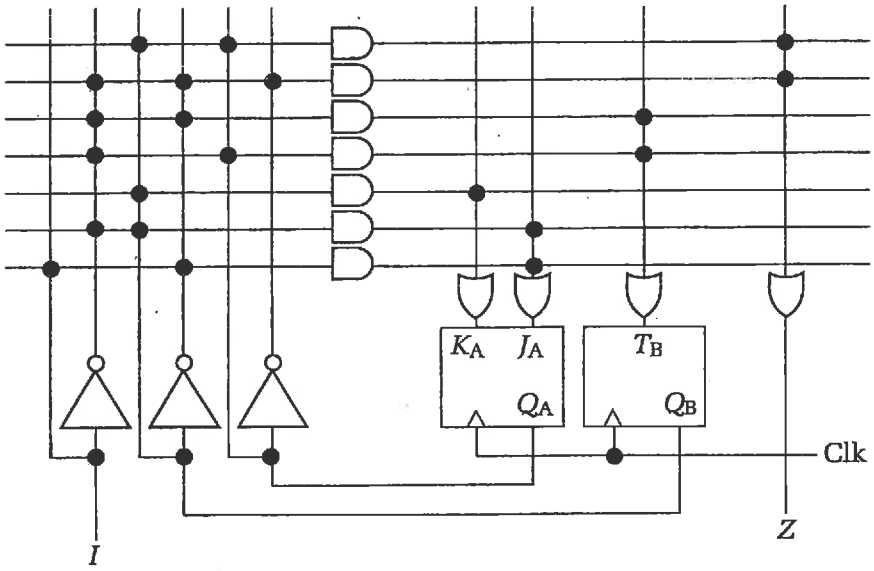
**3.-**The finite state machine (FSM) shown in the figure below is implemented with one toggle (T) flip-flop and one JK flip-flop. It has one input I and one output Z. The combinational logic required for the next state and output functions is implemented by a PLA structure.

(a) Write the logic expressions for $J_A$, $K_A$, $T_B$ and Z.

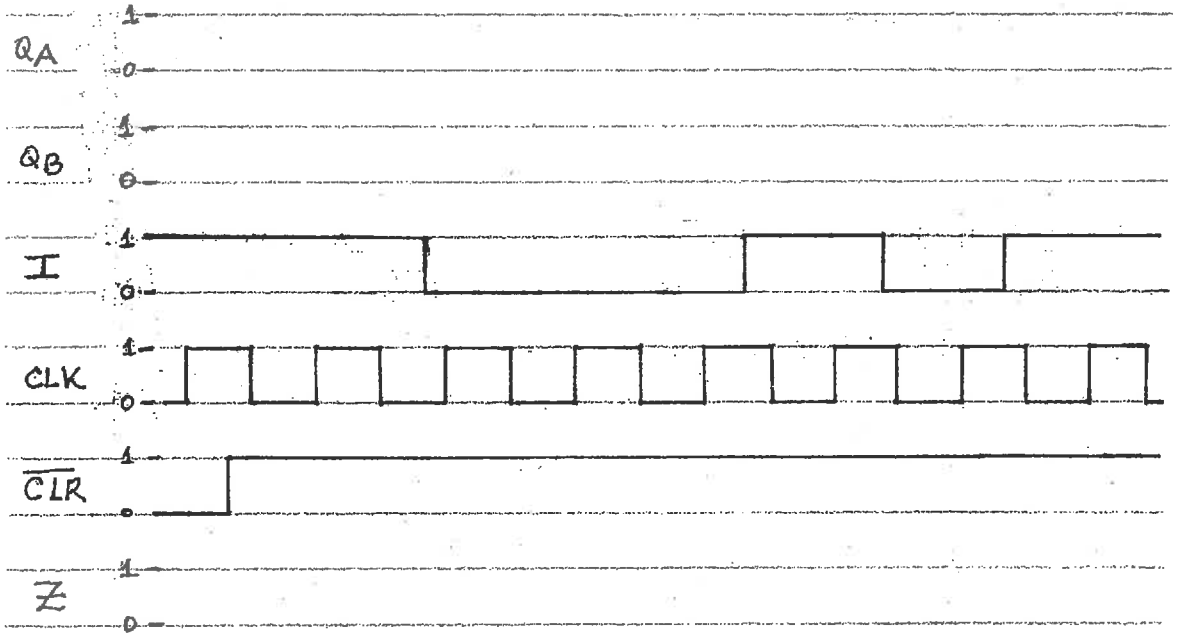
(b) Is this a Moore or a Mealy machine? Explain.

(c) Obtain the state transition table including the output Z.

(d) Draw the complete state transition diagram of the FSM.




(e) Assuming the $\overline{PR}$ is deasserted (HIGH) and the active-low clear $\overline{CLR}$ below is connected to both flip-flops, complete the timing diagram below for $Q_A$, $Q_B$ & Z.




*Note*: Consult flip-flop excitation tables attached at the end as needed.

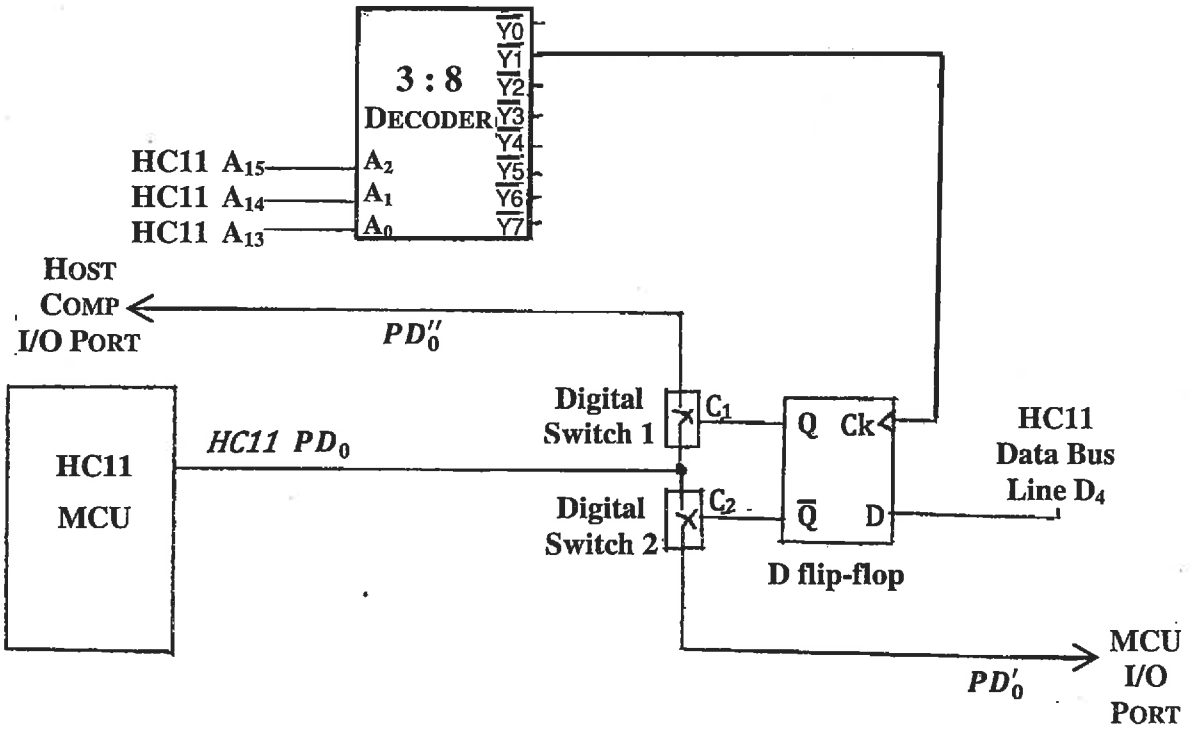
4.- The diagram below shows the use a D flip-flop governing two digital switches in order to route line $PD_0$ of the HC11 microcontroller unit (MCU) to one of two connectors: the HOST computer I/O port or the MCU I/O port connector.
Digital switches close when control input C is at a logic '1' and remain open when C is '0'.
HC11 address lines $A_{15}$ - $A_{13}$ are connected to the 3 address inputs of a 3:8 decoder as shown in the figure, the most significant address input of the decoder is $A_2$ and the least significant is $A_0$. Assume the decoder is enabled and towards the end of the execution of each instruction cycle all its active-low outputs $\bar{Y}_0$ - $\bar{Y}_7$ go back to their inactive logic '1' state.
The data bus line $D_4$ of the HC11 is connected to the flip-flop D input.
Knowing that instruction
**ldaa #$xx** means load HC11 CPU register accumulator A with hexadecimal value xx, and
**staa $zzzz** means store the value in accumulator A to address $zzzz,
which of the following set of instructions will direct HC11 line $PD_0$ to the HOST computer I/O port, which to the MCU I/O port connector and which will not affect the current routing.
Mark your choice with an **X** and justify your selection in each case.

(a) ldaa #$32, staa $3800 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(b) ldaa #$4C, staa $4000 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(c) ldaa #$79, staa $1F00 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(d) ldaa #$8A, staa $2500 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action



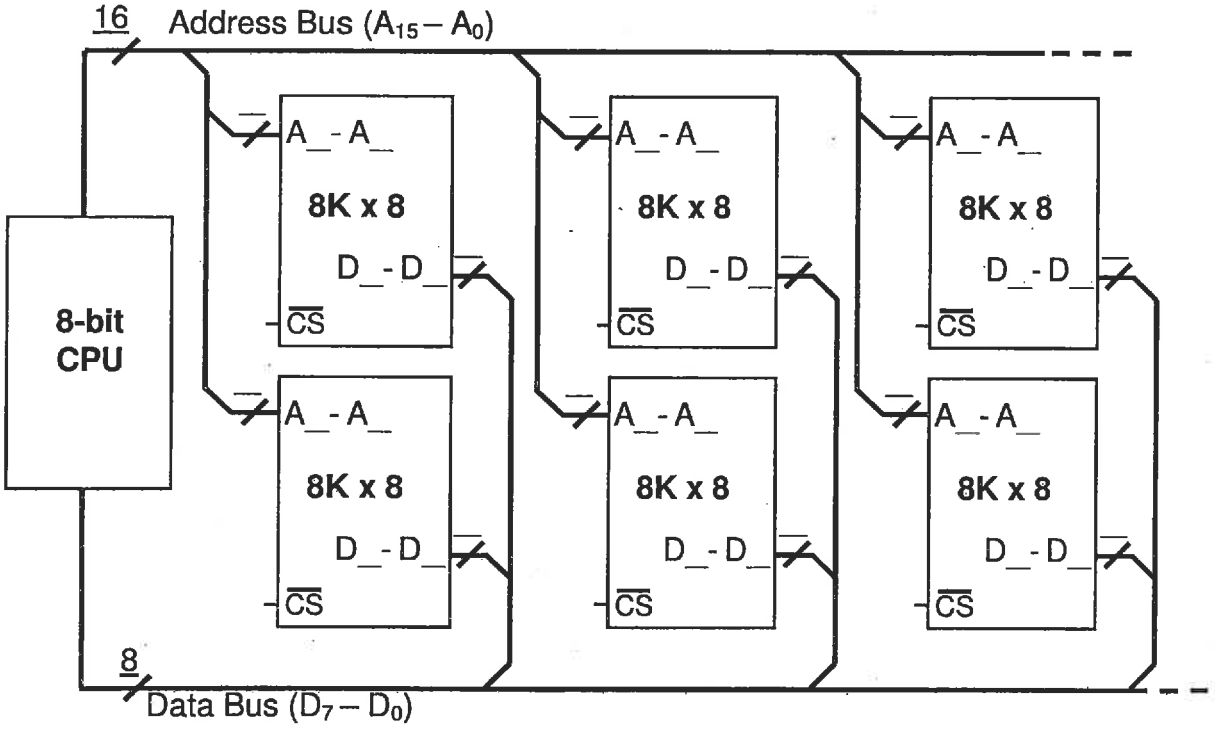
5.- Provide this 8-bit CPU with a 48Kbyte memory space by making use of 8K x 8 memory chips like the ones provided in the figure below. Address range \$0000 – \$3FFF is reserved for other purposes and should be avoided.

(a) Fill in the blanks *beside* and *inside* the memory chips with the appropriate numbers. The number on top of this symbol ⟋ represents the number of lines on that bus. The spaces besides the A's and the D's are to indicate which lines of the address and data busses are connected to each chip, respectively.

(b) Complete the connections in the figure below adding logic gates where needed to produce the chip select (CS) signals needed (the decoding logic). Explain the reasons for the connections made, include expressions for the Boolean logic used. Make sure no duplicity in address exists for any memory location.

(c) Provide the address range allocated to each chip.

Note: R/$\overline{W}$ & clock signals are omitted for simplicity.



**6.-** (a) i. What are the main two types of semiconductor memory?

ii. Mention two differences between them.

(b) i. Mention and describe two methods for communication between the CPU and I/O ports.

ii. Which method is more efficient? Justify.

(c) i. Mention two common CPU registers.

ii. Describe what these two registers are used for.

## Excitation Table

| Q | Q+ | R | S | J | K | T | D |
|---|---|---|---|---|---|---|---|
| 0 | 0 | X | 0 | 0 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | X | 1 | 1 |
| 1 | 0 | 1 | 0 | X | 1 | 1 | 0 |
| 1 | 1 | 0 | X | X | 0 | 0 | 1 |

## Basic Boolean Identities

| | Identity | Comments |
|---|---|---|
| 1. | $A+0=A$ | Operations with 0 and 1 |
| 2. | $A+1=1$ | Operations with 0 and 1 |
| 3. | $A+A=A$ | Idompotent |
| 4. | $A+\overline{A}=1$ | Complementarity |
| 5. | $A\cdot 0=0$ | Operations with 0 and 1 |
| 6. | $A\cdot 1=A$ | Operations with 0 and 1 |
| 7. | $A\cdot A=A$ | Idompotent |
| 8. | $A\cdot\overline{A}=0$ | Complementarity |
| 9. | $\overline{\overline{A}}=A$ | Involution |
| 10. | $A+B=B+A$ | Commutative |
| 11. | $A\cdot B=B\cdot A$ | Commutative |
| 12. | $A+(B+C)=(A+B)+C=A+B+C$ | Associative |
| 13. | $A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$ | Associative |
| 14. | $A\cdot(B+C)=(A\cdot B)+(A\cdot C)$ | Distributive |
| 15. | $A+(B\cdot C)=(A+B)\cdot(A+C)$ | Distributive |
| 16. | $A+(A\cdot B)=A$ | Absorption |
| 17. | $A\cdot(A+B)=A$ | Absorption |
| 18. | $(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$ | Consensus |
| 19. | $\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$ | De Morgan |
| 20. | $\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$ | De Morgan |
| 21. | $(A+\overline{B})\cdot B=A\cdot B$ | Simplification |
| 22. | $(A\cdot\overline{B})+B=A+B$ | Simplification |