National Exams May 2011

07-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   You are required to answer questions 3, 4, 5 and 6.
   You have a choice of answering question 1 or question 2.
   Clearly indicate your choice, otherwise only the first answer found will be marked.

4. Questions 1, 2 and 3 are worth 15 points.
   Questions 4, 5 and 6 are worth 12 points.

Marking Scheme

1. (a) 3, (b) 3, (c) 3, (d) 3, (e) 3, total = 15
2. (a) 3, (b) 6, (c) 6, total = 15
3. (a) 4, (b) 4, (c) 4, (d) 3, total = 15
4. (a) 4, (b) 5, (c) 3, total = 12
5. (a) 4, (b) 4, (c) 4, total = 12
6. (a) 6, (b) 6, total = 12

The number beside each part above indicates the points that part is worth

1.- (i) Given the function f in sum of products form:

$$f(A,B,C) = AB\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B}C$$

(a) Prepare its truth table.

(b) Express f in canonical product of sums (PoS) form.

(c) Use Karnaugh maps (K-maps) to express f in minimized PoS form.

(ii) Given the function g expressed in abbreviated canonical notation as:

$$g(A,B,C,D) = \sum m_i(0,8,9,14,15) + \sum d_i(1,2,6,10,13)$$

where $\sum d_i(\cdots)$ indicate *don't care* combinations.

(d) Map the function g in a K-map and find the minimized sum-of-products (SoP) form.

(e) Is the expression found in part (d) hazard-free?
If it is justify why, or if it is not find the smallest hazard-free SoP form.

2.- Design a converter that maps a 4-bit binary code into a 4-bit Gray code. The 4-bit Gray code sequence is defined as follows: 0000, 0001, 0011, 0010, 0110, 0111, 0101, 0100, 1100, 1101, 1111, 1110, 1010, 1011, 1001, 1000.

(a) Give the truth table.

(b) Find the minimized expressions for the output functions using K-maps.

(c) Show how to implement this code converter as either a PAL or a PLA circuit, whichever you consider more appropriate. Justify your choice.

3.- Design and synthesize a finite state machine (FSM) that has one input X and one output Y. The FSM must use T flip-flops to implement a modulo-8 binary synchronous counter that counts up when X = 1, *e.g.* 000, 001, 010, 011, ..., 111, 000, 001, ..., and counts down when X = 0, *e.g.* 111, 110, 101, 100, ..., 001, 000, 111, ... The active-high output Y must signal when the counter reaches 111 when counting up or when the counter reaches 000 when counting down.

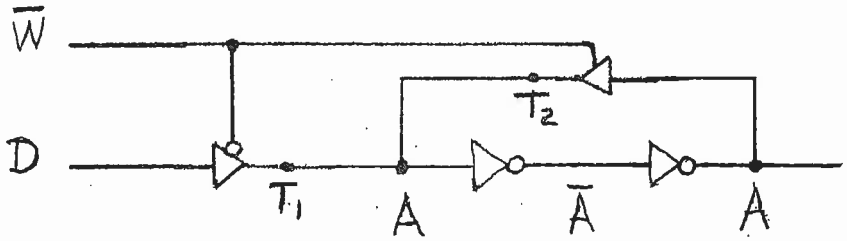
(a) Draw the state transition diagram for the FSM.

(b) Obtain its state transition table including flip-flop inputs, X and Y.

(c) Synthesize the logic circuit implementing the FSM.

(d) Is this a Moore or a Mealy FSM? Justify your answer.

4.- The figure below shows a memory cell A built using two cascaded inverters. Data input D contains the value to be written to the memory cell. Control input $\overline{W}$ (write) determines when the value of the memory cell is to be updated with the value in D. Two tri-state gates (buffers) are used for this purpose.



(a) Is the control input $\overline{W}$ (write) active-low or active-high?
Explain by describing how the value of the cell is (i) held and (ii) updated.

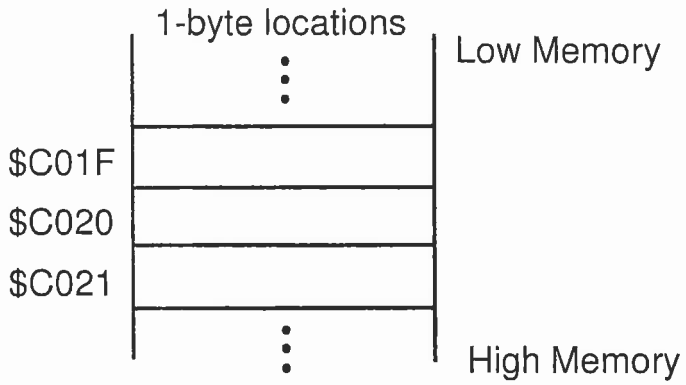
(b) Provide a truth table having A, D and $\overline{W}$ as inputs, and showing the values of the 2 tri-state gate outputs T_1 and T_2 for each input combination.

(c) For how long $\overline{W}$ has to be active for the memory update to be successful? Explain.

5.- For microprocessors, such as Motorola's, that use big-endian order for storing multiple-byte variables

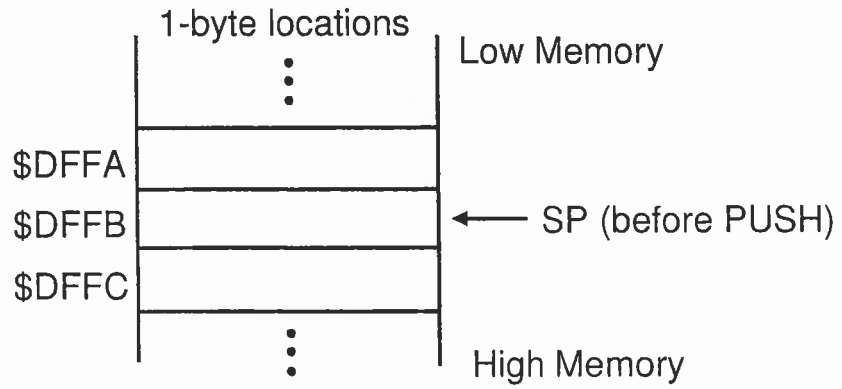
(a) Fill the memory block below with the result of the instruction:

"Store the 16-bit number $3D95 to address $ C020"



(b) The SP = $DFFB. Fill the memory block below with the result of the instruction:

"Push the 16-byte number $3D95 onto the stack"



(c) What is the value of the stack pointer register SP after the PUSH?

6.- (a) i. Using 8K x 4 SRAM memory chips, how many SRAM chips will be needed to build a 16KB (kilobyte), 8-bit memory system for an 8-bit microprocessor?
CPU word size = 8bits.

(a) ii. What is the size of the address bus required by the CPU in order to be able to address this memory space?

(a) iii. What is the size of the data bus?

(b) i. Using 32K x 8 SRAM memory chips, how many SRAM chips will be needed to build a 64KB (kilobyte), 16-bit memory system for a 16-bit microprocessor?
CPU word size = 16bits.

(b) ii. What is the size of the address bus required by the CPU in order to be able to address this memory space?

(b) iii. What is the size of the data bus?

Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot\overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification