National Exams May 2010

04-BS-8, Digital Logic

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made with the answer of the question.

2. Candidates may use one of two calculators, the Casio, or Sharp approved models. This is a closed book examination, however, candidates are allowed to bring the following into the examination room:
   (i) ONE aid sheet 8.5" x 11" hand-written on both sides containing notes and formulae.

3. This paper contains **SIX (6)** questions and comprises **seven (7)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100

6. Each question carries 25 marks and the marks for each question part are indicated in brackets.

7. Data on some relevant Digital ICs are provided in the Appendix.

8. A PAi 16i 8 Data sheet is provided on page 7 (in the Appendix). It can be used to provide the solution of Problem 2, part (b) and should be attached to your answer book.

1. (a) Convert the decimal numbers 147 and 31 to binary by using 8-bit 2's coP SleP ent reSresentDtion Dnd SerIorP the Iollowing oSerDtions:

i) 147 – 31
ii) (-147) + 31
iii) 147 + 31

Convert the answers back to their decimal representation to verify that your answer is correct

(14 marks)

(b) The following is a string of ASCII characters whose bit patterns have been converted into following hexadecimal numbers:
76 c4 EA 73 E5 4A Ec 64 75
In the 8-bits of each hex pair the most significant bit is the parity bit and the remaining seven bits are the ASCII code.

i) Decode the ASCII string into ASCII characters.
ii) Determine the parity type used in the string, i.e. identify the odd or even parity.

(11 marks)

2. Consider a Boolean function **F** given below.

F(w, x, y, z) = **xy'z + x'y'z + w'xy + wx'y + wxy**

(a) r se Boolean algebra to simplify the function and implement it using the minimum number of standard gates.

(8 marks)

(b) Implement the function c on a PAi 16i 8 device. The logic diagram of PAi 16i 8 is given in the Appendix. Show the intact PAi fuses by crossing them in the diagram and attach it to your answer book.

(5 marks)

(c) Implement the minimized form of **F** of part (a) by using only 2-input NOR gates.

(5 marks)

(d) Use K-map method to simplify the function **F** and compare it with the results of part (a).

(7 marks)

3. (a) Briefly answer the following questions:
   i) Explain the difference between a truth table and a state table.
   ii) Identify any relationship between a state table and a state diagram of a sequential circuit.
   iii) Sequential machines are of two types the Moore and Mealy type sequential machines. Generally which type of machines are prune to noise at its inputs. Justify your answer.

(15 marks)

(b) Design a sequential circuit with two D flip-flops and one input x. When x = 0, the state of the circuit remains the same and when x =1, the circuit goes through the state transitions from 00 to 11, to 01, to 10, back to 00, and repeats.

(10 marks)

4. A majority circuit is a combinational logic circuit whose output is logic 1 iI WKe inSuWvDUiDEOes KDve equDORUP RUe 1's WKDn WKe 0's. 7Ke RuWSuWis logic 0 when the number of input variables equal to 0 is less than that equal to 1.

(a) Design a four-input majority circuit (shown in Figure n 4) by finding the truth table, Boolean equations and simplifying the equations. Draw the logic diagram of the circuit.

(15 marks)

(b) Implement the majority circuit by using a suitable size decoder and external gates.

(10 marks)

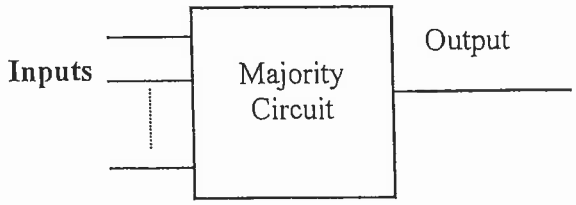


Figure n 4

5. (D) DesiJn D seUDO2's FRP SGeP enWFiUFuiWKDvinJ D sKiIWUeJisWeU DnG D IGS-IGRS. 7Ke EinDUy nuP EeUis sKiIWeG RuWIRUP Rne-siGe DnG iWs 2's complement shifted into the other side of the shift register.

(13 marks)

(b) Design a timing circuit, which provides an output signal that stays active for exactly 6 clock cycles. A start signal sends the output to the 1 state, and after 6 clock cycles the signal returns to the 0 state.

(12 marks)

6. It is required to generate four repeated signals q0 through q3 similar to the ones shown in Figure n6. Design the circuit for this purpose.

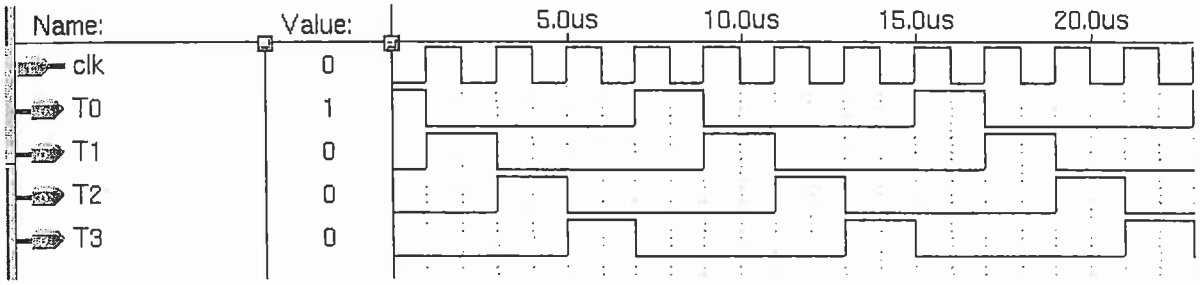


Figure n6

(a) Use flip-flops and some gates to generate q0, q1, q2 and q3 signals.

(14 marks)

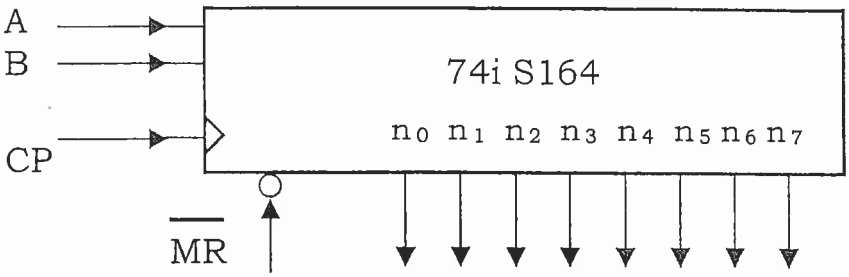
(b) Use a counter and a decoder to generate the same q0 through q3 signals.

(11 marks)

APPENDIX

Some Useful Data Sheets

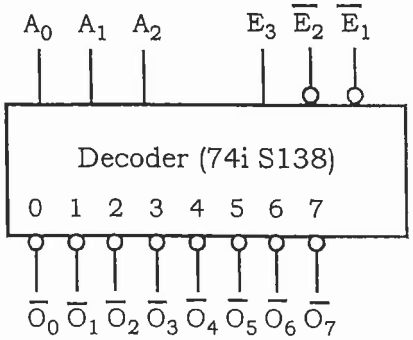
74LS164: 8-bit Shift Register



- An eight-bit shift register with all FF outputs n_0, n_1, n_2, n_3, n_4, n_5, n_6 and n_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop n_0.
- Shift operation occurs at PGqs of the clock input CP.
- qhe $\overline{MR}$ input resets all FFs asynchronously on a i OW level.

Decoder Data Sheet

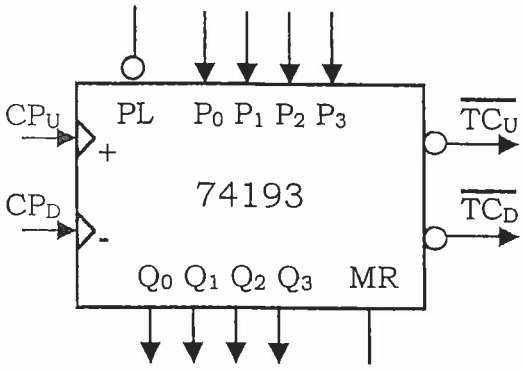
74LS138: 3-to-8 Decoder



Inputs			Outputs
$\overline{E}_1$	$\overline{E}_2$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled - all e IGe
x	1	x	Disabled - all e IGe
x	x	0	Disabled - all e IGe

74193, 4-bit UP/DOWN Counter

MR	$\overline{PL}$	CP_U	CP_D		Mode
e	x	x	x		Asynch Reset
i	i	x	x		Asynch i oad
i	e	e	e		No change
i	e	↑	e		Count up
i	e	e	↑		Count down



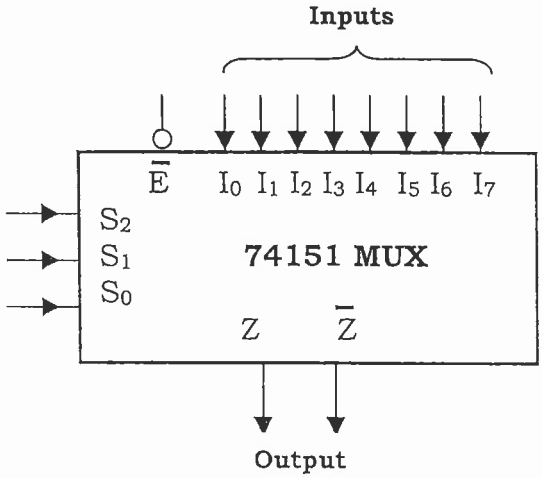
Pins	Description
CP_U	Count-up clock input
CP_D	Count-down clock input
MR	Asynchronous master reset input
$\overline{PL}$	Asynchronous parallel load input
P_0-P_3	Parallel data inputs
Q_0 - Q_3	Flip-flop outputs
$\overline{TC_U}$	Terminal count-up (carry) output
$\overline{TC_D}$	Terminal count-down (borrow) output

Multiplexer Data Sheet

74151 8-to-1 Multiplexer

Inputs Outputs

$\overline{E}$	S_2	S_1	S_0		Z	$\overline{Z}$
H	x	x	x		H	L
L	L	L	L		$\overline{I_0}$	I_0
L	L	L	H		$\overline{I_1}$	I_1
L	L	H	L		$\overline{I_2}$	I_2
L	L	H	H		$\overline{I_3}$	I_3
L	H	L	L		$\overline{I_4}$	I_4
L	H	L	H		$\overline{I_5}$	I_5
L	H	H	L		$\overline{I_6}$	I_6
L	H	H	H		$\overline{I_7}$	I_7



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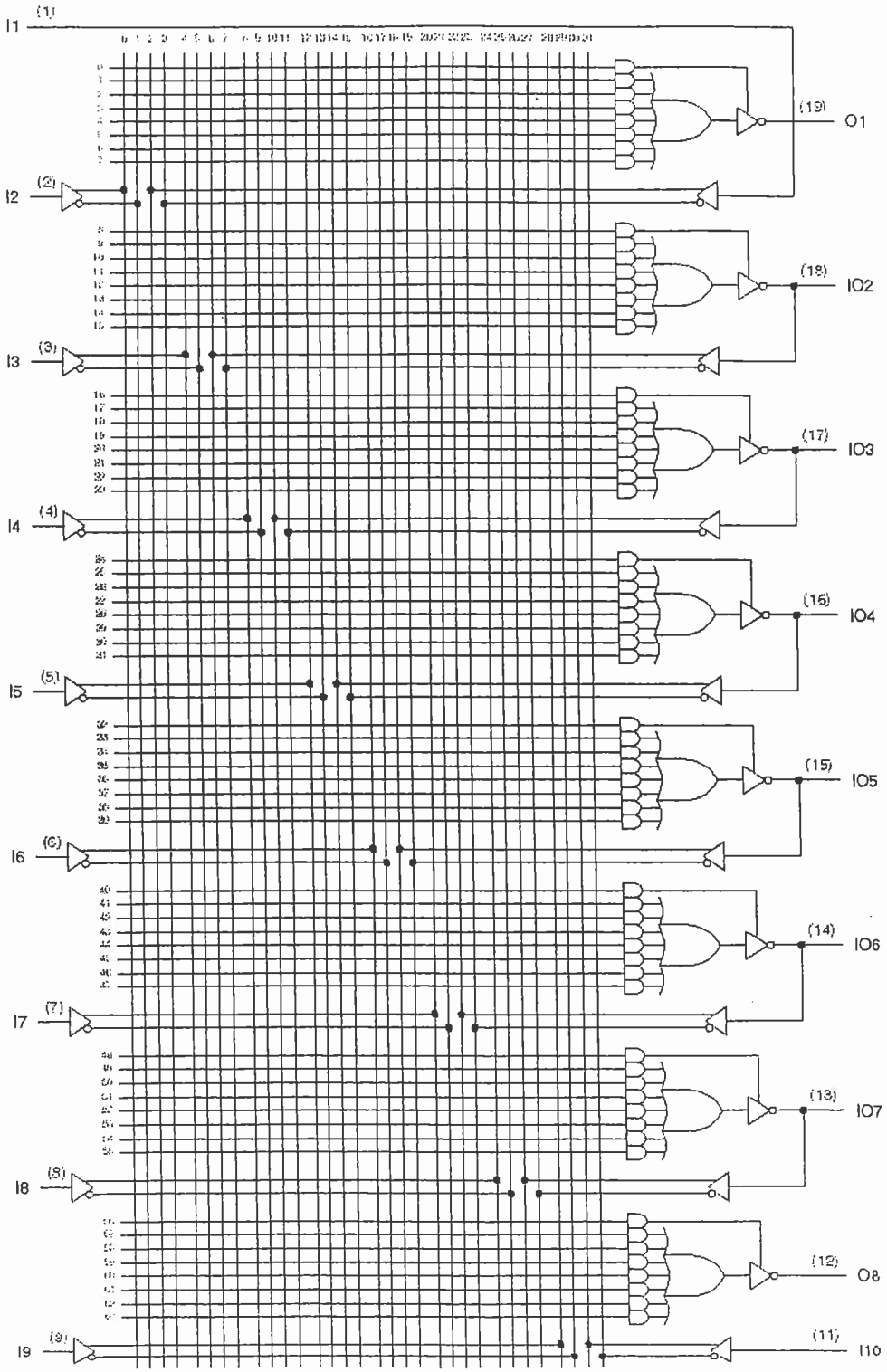

END OF Paper

Marking Scheme

1. 25 Marks Total
   (a) 14 marks
   (b) 11 marks

2. 25 Marks Total
   (a) 8 marks
   (b) 5 marks
   (c) 5 marks
   (d) 7 marks

3. 25 Marks Total
   (a) 15 marks
   (b) 10 marks

4. 25 Marks Total
   (a) 15 marks
   (b) 10 marks

5. 25 Marks
   (a) 13 marks
   (b) 12 marks

6. 25 Marks Total
   (b) 14 marks
   (b) 11 marks