National Exams December 2010

98-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.

2. This is a CLOSED BOOK exam.
   A Casio or Sharp approved calculator may be used.

3. FIVE (5) questions constitute a complete exam paper.
   The first 5 questions as they appear in the answer book will be marked.

4. Each question is of equal value.

Question 1 (20 marks)

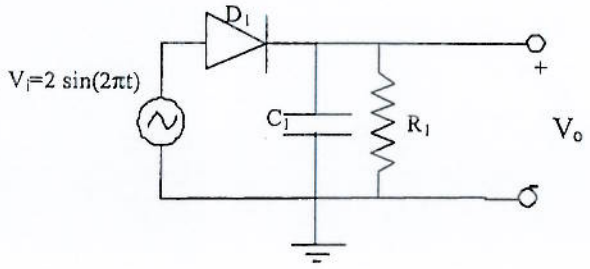

Figure 1. The diode is ideal. R_1=50Ω, C_1=10 μF.

For the circuit shown in Figure 1:

a) Sketch V_i and V_o as a function of time, indicating peak voltages.

b) What is the amplitude of the ripple in V_o?

c) What is the peak inverse voltage across the diode?

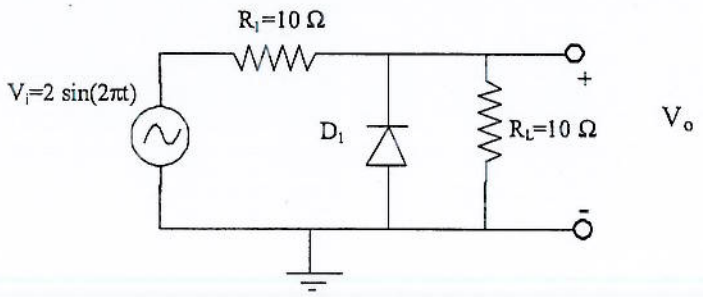

Figure 2. Assume the diode can be replaced by piece-wise linear model with V_D=0.7V, R_S=1Ω when forward biased.

For the circuit shown in Figure 2:

d) Sketch V_o as a function of time, indicating peak voltages.

e) What is the peak current through the diode?

Question 2 (20 marks)

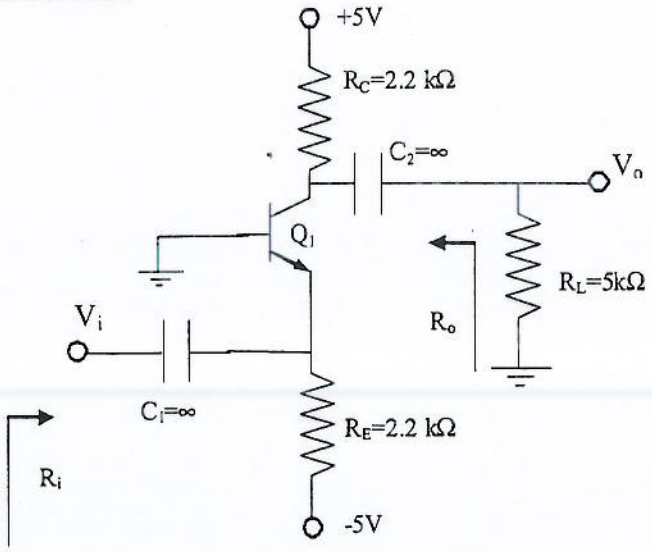

Figure 3. β=100

For the circuit shown in Figure 3:

a) Calculate the dc bias point, indicating V_E, V_C, I_E, I_C, and I_B for the transistor.

b) Draw a small signal ac equivalent circuit. Note that you may wish to use a T model.

c) Find the voltage gain V_o/V_i.

d) Find the input resistance R_i, as indicated in the Figure.

Question 3 (20 marks)

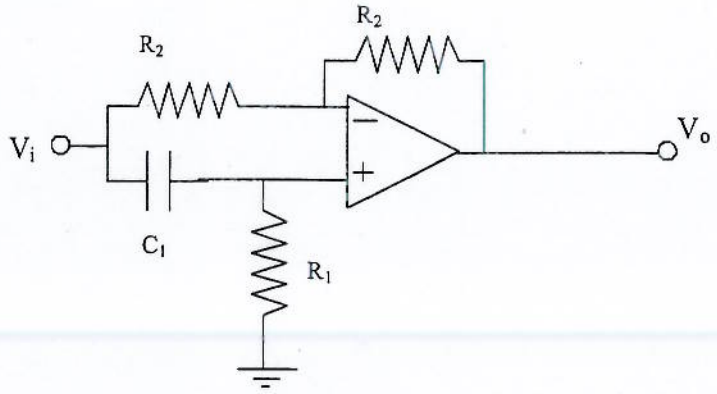

Figure 4.

For the circuit shown in Figure 4:

a) Derive the transfer function $\frac{V_o(s)}{V_i(s)}$, assuming the op-amp is ideal.

b) Find an expression for the phase $\phi(\omega)$.

c) Sketch a Bode plot of the magnitude of the transfer function, showing all the important features.

d) Sketch a Bode plot of the phase of the transfer function, showing all the important features.

Question 4(20 marks)

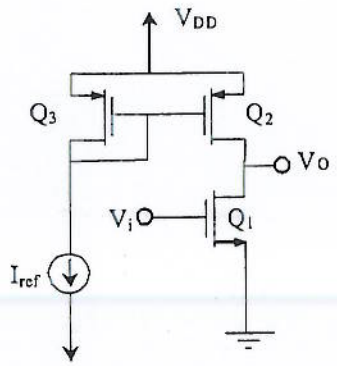

Figure 5. K_n=50 μA/V^2, K_p=20 μA/V^2 V_{tn}=-V_{tp}=1V, V_{DD}=5V, I_{ref}=100 μA, $|V_A|$=100V, W/L=10μm/2μm.

For the circuit shown in Figure 5:

a) Explain the function of each transistor in this circuit.

b) Draw the AC small signal equivalent model for this circuit.

c) Find the output resistance.

d) Find the voltage gain.

e) If the circuit was modified so that the gate of Q1 was grounded and the input signal was applied to the source of Q1, explain how the body effect would be included in your analysis.

Question 5 (20 marks)

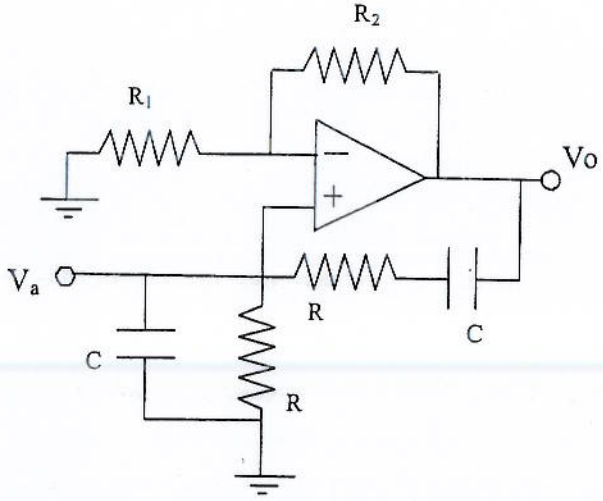

Figure 6. Assume the op-amp is ideal and can provide ±15 V output. R=10kΩ, C=10 nF, R_1=10kΩ, R_2=20kΩ.

For the circuit shown in Figure 6:

a) Find an expression for the loop gain.

b) What is the condition for oscillation, and at what frequency does this occur?

c) What is the amplitude of the circuit output? How can you change the amplitude?

Question 6 (20 marks)

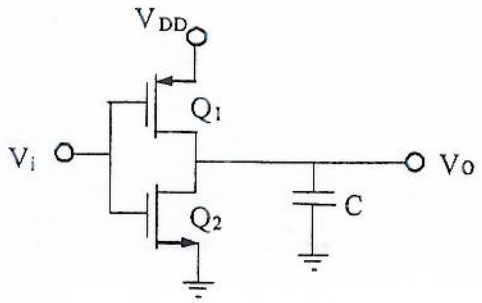

Figure 7. K_n=50 μA/V^2, K_p=20 μA/V^2 V_{tn}=-V_{tp}=1V, $(W/L)_n$=2μm/1μm, V_{DD}=5V, C=100fF.

For the circuit shown in Figure 7:

a) Choose a size $(W/L)_p$ to provide a symmetrical transfer characteristic.

b) If V_i switches from high to low, find the initial current drawn from V_{DD}.

c) Estimate the time required for this circuit to switch states.

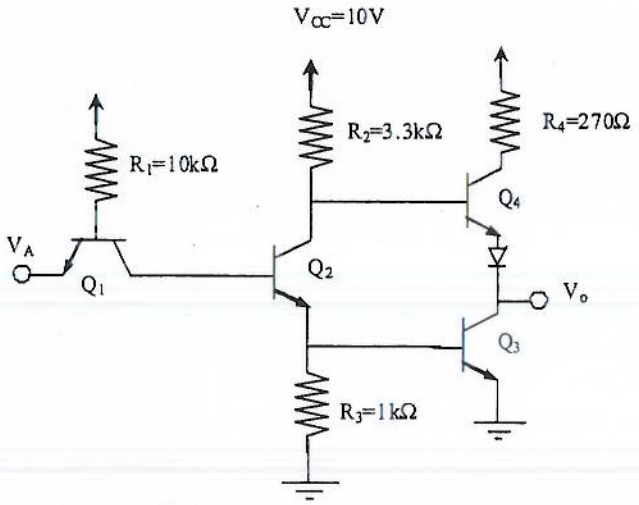

Figure 8. β is very large, V_{BE}=0.7V (active), V_{CC}=10V.

For the circuit shown in Figure 8:

d) This basic TTL gate has 3 stages. Identify them and explain their function.

e) If the input V_A is high (+5V) how much current is drawn from V_{CC}?

Question 7 (20 marks)

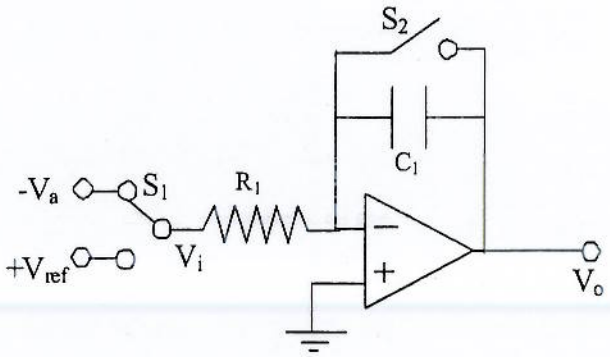

Figure 9. Assume the op-amps are ideal. Supply voltages are +/-10V.

For the circuit shown in Figure 9, for $t<0$ S_2 is closed. At $t=0$ S_2 is opened, S_1 is connected to $-V_a$. At $t=t_1$ S_1 is connected to $+V_{ref}$ and S_2 remains open.

a) What is the expression for the output $V_o(t)$?

b) Sketch the output V_o as a function of time indicating peak values and slopes.

c) Explain how this circuit could be incorporated in an analog to digital converter.

d) What determines the resolution of this type of converter?

e) Describe the operation of a simple digital to analog converter using binary weighted resistors, and sketch a possible circuit implementation.