National Exams December 2010

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination, however, candidates are allowed to bring the following into the examination room:
   (i) One hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **SIX (6)** questions and comprises **seven (7)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and the marks for each question part are indicated in brackets.

7. Data of some relevant Digital ICs are provided in the Appendix.

8. A PAL16L8 Data sheet is provided on page 7 (in the Appendix). It can be used to provide the solution of Problem 2, part (b) and should be attached to your answer book.

1. A combinational logic circuit with two outputs **F1** and **F2** needs to be implemented. The output functions **F1** and **F2** are given below:

   F1(w, x, y, z) = $\sum$**m**(0, 2, 4, 6, 7, 9) + **D**(10, 11)

   F2(w, x, y, z) = $\sum$**m**(2, 4, 9, 10, 15) + **D**(0, 13, 14)

   (a) Design the minimum-cost logic circuit for both functions and draw the combined circuit. Compare the cost of the combined logic circuit with the total cost of two individual circuits that implement functions **F1** and **F2** separately.

   (12 marks)

   (b) Identify the main differences between FPGA and PAL devices.

   (5 marks)

   (c) Implement the minimum-cost circuit of part (a) on a PAL16L8 device. The logic diagram of PAL16L8 is given in the Appendix. Show the intact PAL fuses by crossing them in the diagram and attach it to your answer book.

   (8 marks)

2. Consider a Boolean function **F** given below.

   F(w, x, y) = **(w + x + y) . (w + x' + y) . (w' + x' + y) . (w + x + y')**

   (a) Use Boolean algebraic manipulation to find the minimum product-of-sum expression of the function **F.** Implement the function using the minimum number of standard gates.

   (9 marks)

   (b) Implement the function **F** by employing the minimum number of AND gates and only one OR gate.

   (10 marks)

   (c) Implement the minimized form of **F** of part (a) by using only 2-input NAND gates.

   (6 marks)

3. (a) Briefly answer the following questions:
   i) Identify the difference between 1's complement and 2's complement representation. Identify any advantages of each of the representation.
   ii) Identify the difference between ripple-carry adder and carry look ahead adder circuits. Describe any reason why a ripple-carry adder takes more time to add as compared with a carry look-ahead adder.
   iii) Determine a BCD representation for $(16,000)_{10}$ number. Justify your answer.

(9 marks)

(b) Determine the number of gates required to implement a 4-bit ripple-carry adder. Use AND, OR and XOR gates only with any number of inputs.

(8 marks)

(c) Show how the function **f** can be implemented using a 3-to-8 binary decoder and an OR gate.

$$\mathbf{f}(x1, x2, x3) = \sum \mathbf{m}(0, 2, 3, 5, 6)$$

(8 marks)

4. Design a synchronous sequential circuit that checks a serial 8-bit data for even parity. The circuit should have two inputs SYNC and DATA in addition to CLOCK and one Moore type output, ERROR as shown in Figure Q4.

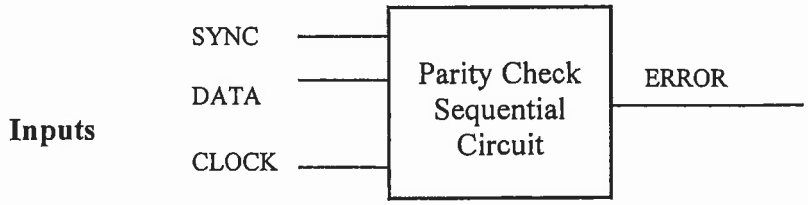


Figure Q4

(a) Derive a State/Output Diagram and Table that does the job by using the minimum number of states.

(13 marks)

(b) Design and implement the Parity Check circuit by using either D flip-flops or J-K flip-flops.

(12 marks)

5. A combinational lock synchronous sequential machine needs to be designed and implement that activates an "unlock" output when a certain binary input sequence is received.

The sequential circuit has one input, X and two outputs, UNLOCK and HINT. The UNLOCK output should be 1 if and only if X is 0 and the sequence of inputs received on X at the preceding six clock ticks was 011011. The HINT output should be 1 if and only if the current value of X is the correct one to move the sequential machine closer to being in the unlocked state with (UNLOCK = 1)

(a) From the above problem description, identify the type of sequential machine (Moore or Mealy). Justify your answer.

(5 marks)

(b) Draw the state/output diagram and table of the sequential machine with the minimum number of states.

(12 marks)

(c) Develop the output equations for UNLOCK and HINT signals of the circuit and identify the number of the flip-flops required for implementing the sequential machine.

(8 marks)

6. Given the logic diagram of Figure Q6 given below:

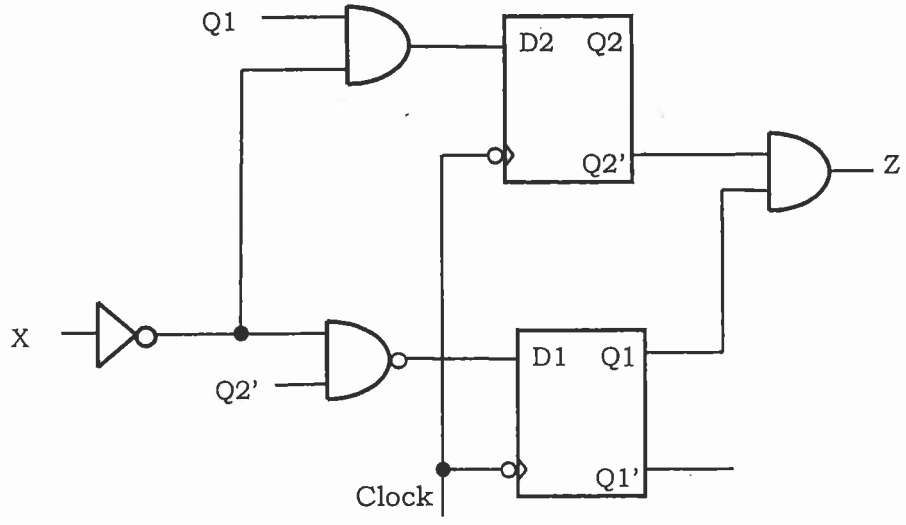


Figure Q6

Question No. 6 continues on Page 5

(a) Derive the excitation and output equations.

(8 marks)

(b) Write down the next state equations and construct the transition table.

(10 marks)

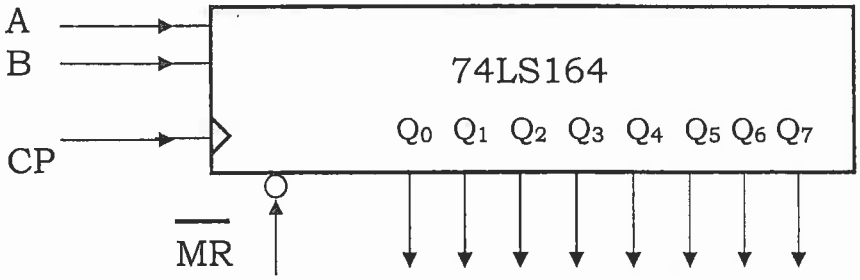
(c) Draw the state diagram for the logic circuit of Figure Q6.

(7 marks)

APPENDIX

Some Useful Data Sheets

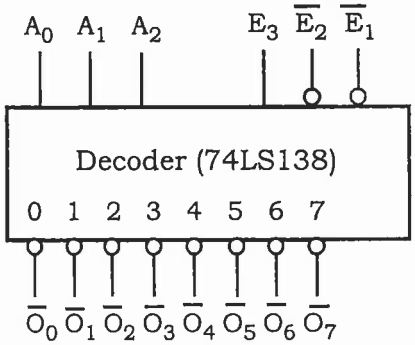
74LS164: 8-bit Shift Register



- An eight-bit shift register with all FF outputs Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0.
- Shift operation occurs at PGTs of the clock input CP.
- The $\overline{MR}$ input resets all FFs asynchronously on a LOW level.

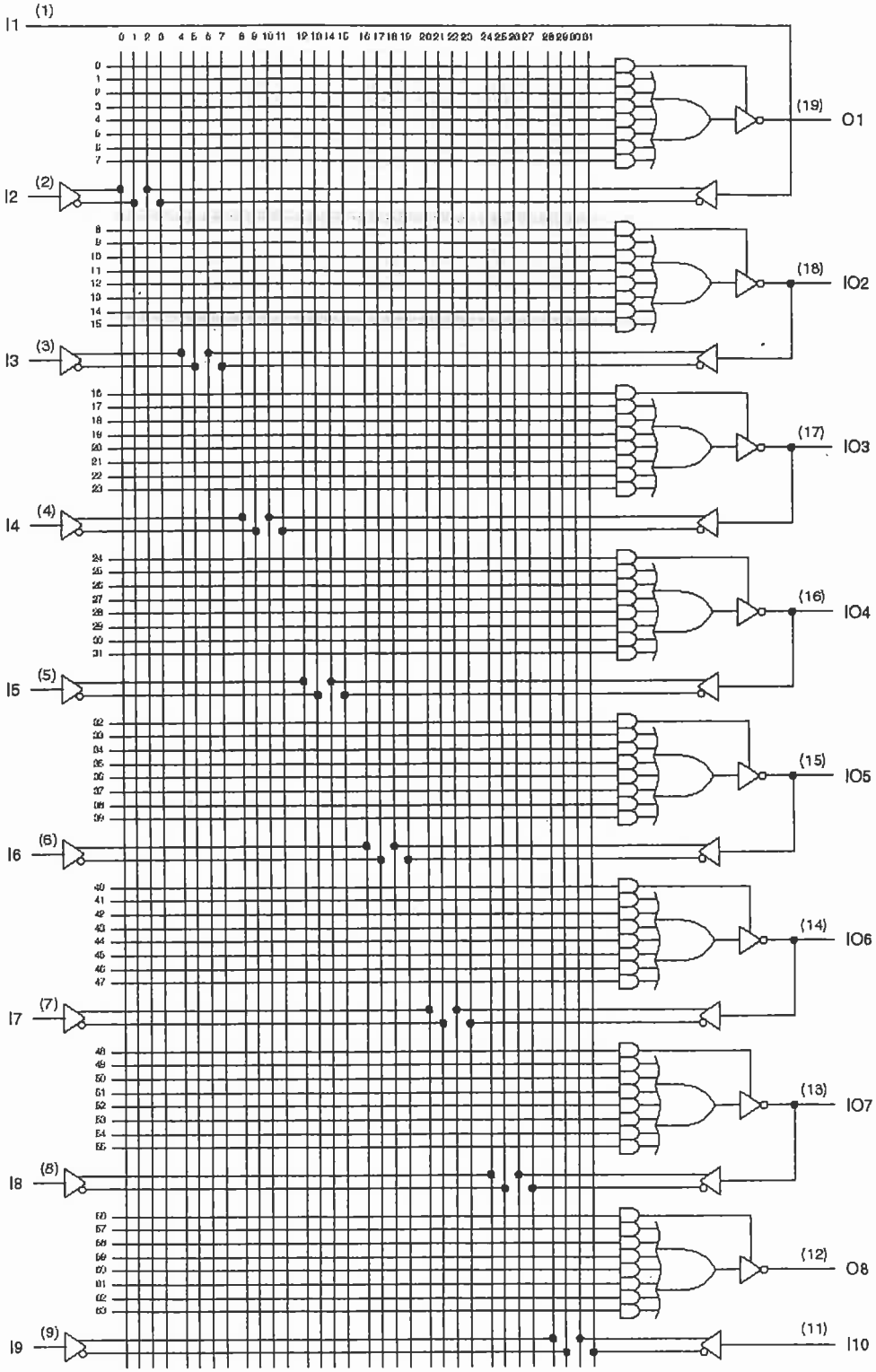
Decoder Data Sheet

74LS138: 3-to-8 Decoder



Inputs			Outputs
$\overline{E}_1$	$\overline{E}_2$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled - all HIGH
x	1	x	Disabled - all HIGH
x	X	0	Disabled - all HIGH

PAL16L8



END OF Paper

Marking Scheme

1. 25 Marks Total
   (a) 12 marks
   (b) 5 marks
   (c) 8 marks

2. 25 Marks Total
   (a) 9 marks
   (b) 10 marks
   (c) 6 marks

3. 25 Marks Total
   (a) 9 marks
   (b) 8 marks
   (c) 8 marks

4. 25 Marks Total
   (a) 13 marks
   (b) 12 marks

5. 25 Marks
   (a) 5 marks
   (b) 12 marks
   (c) 8 marks

6. 25 Marks Total
   (a) 8 marks
   (b) 10 marks
   (c) 7 marks