National Exams, May 2009

98- Comp- A2
Digital Systems Design

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made.

2. This is CLOSED BOOK exam. Only an approved calculator (non-programmable, non- communicating) is permitted.

3. Any FOUR (4) questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

4. Each question is of equal value. Marks for multipart questions are stated in each part.

Question 1 (25 Marks)

A system must be designed to accept three inputs and a clock and provide three outputs. The three inputs are numbered X1, X2 and X3 respectively. The outputs are Y1, Y2 and Y3. Input X1 has higher priority than X2, which in turn has higher priority than X3. Note that Y1 is associated with X1, Y2 is associated with X2 and Y3 is associated with X3. The system must do the following:

do forever {

1. At the positive edge of the clock, check to see that each input is now the same value as it was just prior to the clock edge.
2. If at least one input has changed state from 0 before the positive clock edge to 1 after the positive clock edge, then
   - i. wait for the next positive clock edge
   - ii. on the next positive clock edge, pulse the output corresponding to the highest priority input high for one clock cycle

} loop

For example, the following sequence of inputs will yield the corresponding outputs. Note that the bits to the left are the oldest bits, the bits on the right are the most recent. The rightmost column contains the current signals. **Note that each column corresponds to the state of the three inputs and outputs just after the positive clock edge.**

X1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	0	1	0	1
X2	0	0	0	1	1	0	0	0	0	1	0	1	0	1	1	0	0	1	1	0	0	0	0	1	0	1	0	0	1	0
X3	0	0	0	1	0	1	0	1	1	1	0	0	0	1	1	0	1	0	0	1	1	1	0	1	1	0	0	0	0	0
Y1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	1	0
Y2	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1
Y3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0

oldest   most recent

Design the system. Try to minimize the number of states used and the number of gates and flip-flops used. Use D flip-flops.

Question 2 (25 Marks)

a) (10 Marks) Sketch a block diagram of the datapath for a simple, non-pipelined central processor. Label the various blocks and show the control

signals. Now indicate how the "add r4 $2134" instruction would be executed.

b) **(10 Marks)** If the processor is pipelined, how does this affect the block diagram? How does it change the way that the datapath processes information? Explain with an example.

c) **(5 Marks)** In a pipelined machine, considerable attention is given to branch prediction. Why?

Question 3 (25 Marks)

a) **(15 Marks)** Microprocessors are embedded in an incredibly large number of products today. Each of these systems must be able to interact with the world around it through input/output operations. However, the designer must ensure that the microprocessor will be reliable with all combinations and permutations of its inputs and outputs. Discuss how the designer can do this, from the two perspectives of software and hardware design. What is the major issue and how can the designer minimize it?

b) **(5 Marks)** What are the differences between vectored interrupts and polled interrupts? What are the advantages and disadvantages of each type of interrupt?

c) **(5 Marks)** Key issues that must be addressed in the design of a system with multiple interrupt sources include the length of the Interrupt Service Routines, latency and nesting. Briefly explain each issue and why it is important.

Question 4 (25 Marks)

a) **(15 Marks)** You want to connect together two embedded computers, machine A and machine B, that are 10 cm apart, and choose to do it by connecting together their parallel ports. Machine A will pass 8-bit bytes to machine B using the parallel ports. What other control signals are required to ensure that each byte is passed correctly, and is read exactly once by machine B? What is the protocol that you would use? Explain how the protocol functions.

Note that we do not know when each byte is to be passed to machine B by machine A. Also assume that each machine has other work to do as well. Assume that the two machines are nominally compatible.

b) **(5 Marks)** What hardware issue could arise in part a) of this question that would cause data to be corrupted? Assume that the two machines are nominally compatible.

c) **(5 Marks)** What other ways are there of connecting the machines? What are the advantages and disadvantages of the other methods?

Question 5 (25 Marks)

a) **(10 Marks)** An embedded system based on a microprocessor is being designed to have a 24-bit address bus with a linear address range. The memory is not organized in banks. The system must have ROM from addresses $d00000 to $ffffff, RAM from $000000 to $00ffff, and four I/O devices occupying 16 bytes each anywhere in the address range from $100000 to $17ffff. The system will never be expanded.

The ROM is made up of devices that store 512 KBytes x 8-bits each, the RAM consists of parts that store 128 Kbytes each, and the I/O devices occupy 16 consecutive bytes each.

Design an address decoder for this system. Use as few gates as possible. Note that all devices use active-low chip-select inputs.

b) **(10 Marks)** A typical microprocessor has a bus architecture. The two most-often used bus structures are the von Neumann architecture and the Harvard architecture. Briefly describe each of these and explain the strengths and weaknesses of each.

c) **(5 Marks)** What must a microprocessor do when its RESET input is changed from the asserted state to the de-asserted state? Discuss all of the steps at a high level of detail.