National Exam December, 2009

07-Elec-A1 Circuits

3 hours duration

NOTES:

1. **No questions to be asked.** If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any logical assumptions made.

2. Candidates may use one of two calculators, a Casio or Sharp approved models.

3. This is a **closed book** examination.

4. Any **five questions** constitute a complete paper. Please indicate in the front page of your answer book which questions you want to be marked. If not indicated, only the first five questions as they appear in your answer book will be marked.

5. All questions are of equal value.

6. **Laplace Table** and other useful equations are given in the last page of this question paper.

Marking scheme

Q1: (a)10, (b) 10

Q2: (a) 12, (b) 8

Q3: (a) 15, (b) 5

Q4: (a) 12, (b) 2, (c) 6

Q5: (a) 12, (b) 8

Q6: (a) 10, (b) 10

Q1: For the circuit shown in Figure-1, calculate (a) the voltage V_1 (voltage across the 300Ω resistance), and (b) current through the 15V source. Use Node Voltage analysis. [10+10]

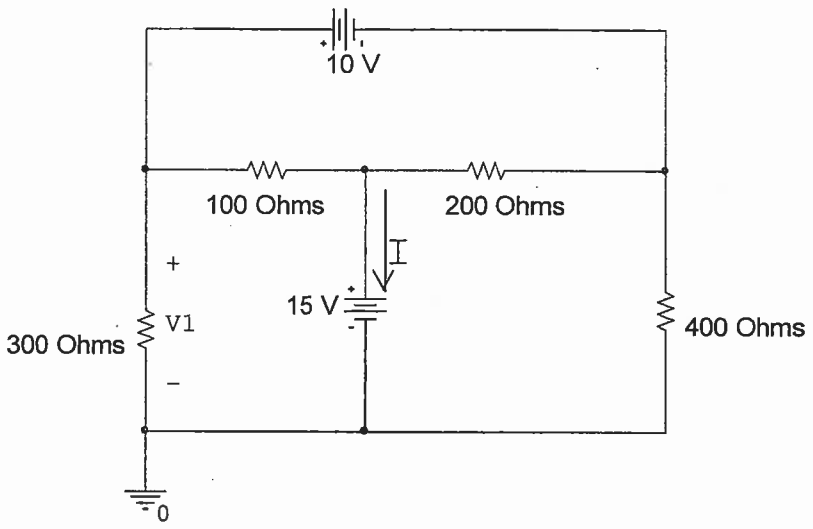

Figure-1

Q2: The switch in Figure-2 was closed for a long time. At t = 0, the switch is opened. (a) Solve the capacitor voltage, $v_c(t)$. (b) Calculate the capacitor voltage at 9ms. [12+8]

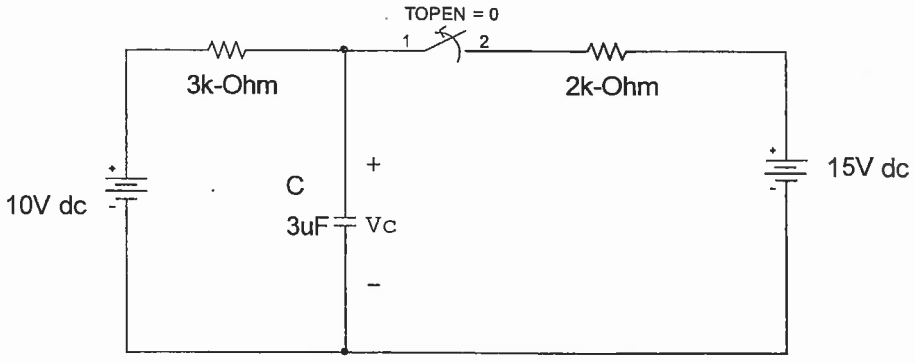

Figure-2

Q3: (a) Use Mesh current analysis and calculate the current, **I** through the inductor of the circuit shown in Figure-3. (b) What is the RMS value of the current, **I** ?

[15+5]

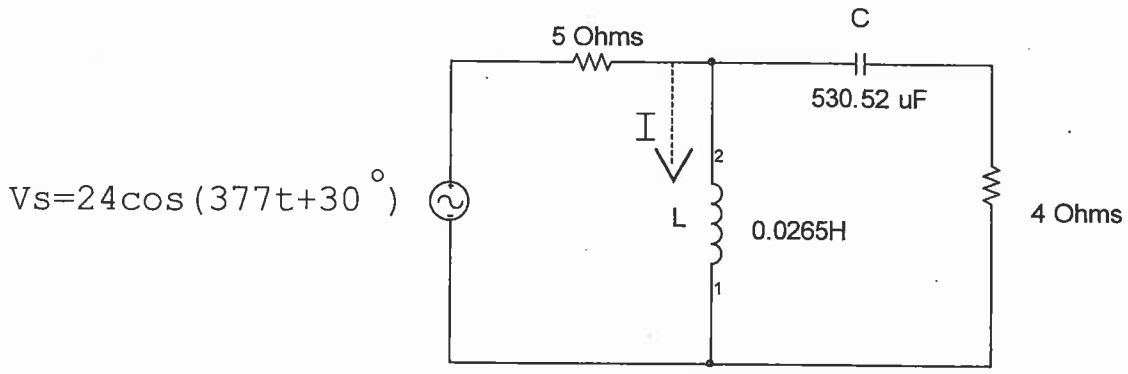

Figure-3

Q4: (a) Thevenize the circuit at terminals **a-b** as shown in Figure-4.

(b) What should be the load impedance, Z_L for maximum power transfer ?

(c) What is the maximum power that can be transferred to load Z_L ?

[12+2+6]

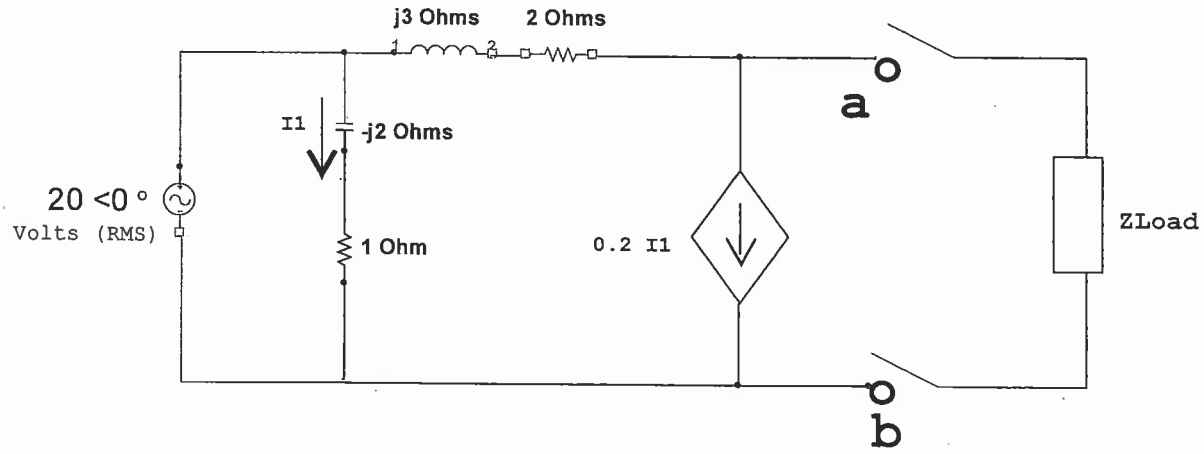

Figure-4

Q5: In the single phase circuit shown in Figure-5, Load1 is 10kW at 0.8 power factor lagging, Load2 is 15kVA at 0.6 power factor lagging.

(a) Calculate the supply current, I_S and the power factor of the supply. [8+4]

(b) What capacitor, C should be connected in parallel to the loads to improve the power factor of the whole load to 0.9 power factor lagging ? [8]

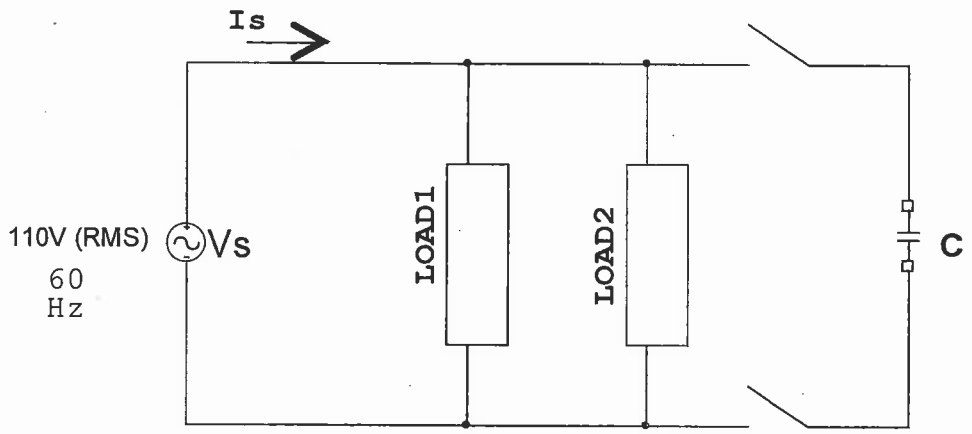

Figure-5

Q6: The circuit shown in Figure-6, the initial inductor current, $i_L(0-) = -1A$, and the initial voltage of the capacitor, $v_c(0-) = 5V$. The switch is closed at $t = 0$.

(a) Draw the Laplace Transformed circuit at $t \geq 0$. [10]

(b) Solve the capacitor voltage, $v_c(t)$ at $t \geq 0$ from the Laplace Transformed circuit. [10]

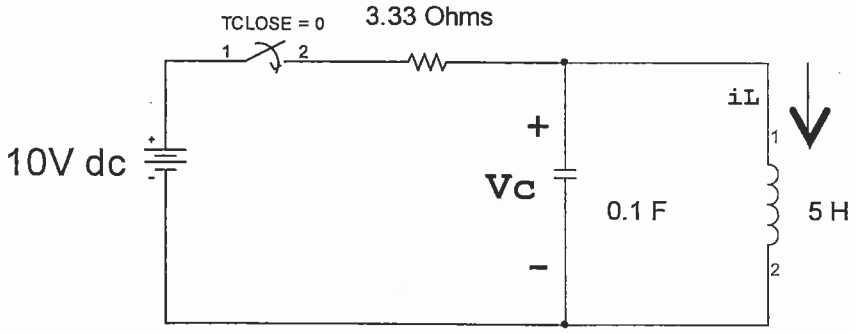

Figure-6

Appendix

Some useful **Laplace Transforms:**

f(t)	→	F(s)
Ku(t)		K /s
e^{-at} u(t)		1 / (s+a)
sin wt .u(t)		w / (s^2+w^2)
cos wt . u(t)		s / (s^2+w^2)
$\frac{df(t)}{dt}$		s F(s) – f(0$^-$)
$\frac{d^2 f(t)}{dt^2}$		s^2F(s) – s f(0$^-$) –f^1(0$^-$)
$\int_{-\infty}^{t} f(q)\,dq$		$\frac{F(s)}{s} + \int_{-\infty}^{0} f(q)\,dq$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}$$